Design of 26GHz Cascode Low Noise Amplifier for 5G Wireless Applications on 0.18µm CMOS Technology

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***Abstract*- Low noise amplifier is an important component of front-end receiver as it amplifies the gain of circuit without degrading its noise figure. This paper presents a modified low noise amplifier composed of three stages: common source followed by 1st and 2nd cascode stage, and it is operating at 26GHz of K-band, this band is generally used for 5G wireless communication. Here, an extra cascode stage is used to improve the gain of overall circuit. In the Proposed circuit of low noise amplifier, S_{11} is -11.29dB, S_{12} is -83.7dB, S_{22} is -9.5dB and gain is 27.31dB whereas noise figure obtained is 2.21dB. Modified Cascode stage is compared with existing cascode stage and there is 8% improvement in gain. This modified circuit is designed and simulated on cadence virtuoso software using 180nm technology and it is biased on 1.8V power supply and 0.8V input voltage is used as input voltage for first stage of circuit.**

***Keywords*- Cadence virtuoso software, Cascode stage, Low noise amplifier, Wireless communication, 5G**

I. INTRODUCTION

Low noise amplifier is first active component on the RF receiver, and it plays important role in improving the overall performance of transceiver. Here, in this paper, a cascode low noise amplifier is presented for improving the gain of the system while maintaining the possible minimum noise figure for the circuit. This low noise amplifier works at 26GHz which is generally used for line-of-sight wireless communication and satellite communication. This frequency was picked up for IMT at WRL19 and now this landmark decision leads national government across the world have the chance to use this frequency for 5G Networks and this decision can provide long lasting benefits for society. Frequency band of 26GHz to 40GHz is most likely band to enable the ultra-high-speed vision for 5G.

Here main challenge is to designing low noise amplifier having 50ohm impedance matching with acceptable noise and improved gain factor. Now-a-days, Researchers are using various technologies to improve the performance of circuits, by using different composition of semiconductor material in transistor manufacturing, like gallium nitride (GaN) material can improve the overall gain of circuit [7].

In paper [3], Low noise amplifiers are designed for two different frequencies i.e., 24GHz and 26GHz and their overall performance has been compared. They are simulated and analysed on Advanced design system (ADS) software using 180 nm technology. This paper presents a LNA has three stages that improves the gain of circuit and gain obtained by 24GHz and 26GHz LNAs are 12.86 dB and 8.6 dB, respectively.

In paper [7], a LNA has been designed on different software operating on 26 GHz. This low noise amplifier is simulated and analysed on ADS software. This LNA is designed for 5G applications and it consists of two stages: common source and one cascode stage with LC feedback in first stage that reduces the overall noise figure of circuit, and in second stage, a cascode topology is added to improve the gain of circuit and the gain obtained by circuit is 17.106 dB. This LNA circuit is designed on 180nm technology, and it takes 1.8V as a supply voltage.

In [1], in this paper, same LNA has been designed with extra resistive feedback in cascade stage to suppress the noise of the overall circuit. This low noise amplifier is simulated on cadence virtuoso software on 180nm CMOS technology. This circuit has better gain but with small increment in noise figure. This LNA has also improved the performance of circuit in terms of input and output reflection coefficient, and overall performance has been optimized.

In this paper, three stage LNA is designed to improve the gain of circuit, three stages consist of common source stage, 1st cascode stage and 2nd cascode stage with input and output matching networks. This low noise amplifier has been simulated and analysed on cadence virtuoso software on 180nm technology and supply voltage of 1.8V and 0.8V given as input voltage to bias the first stage of circuit.

This proposed circuit has its peak value in K- band and the basic block diagram of the circuit is shown in figure.1

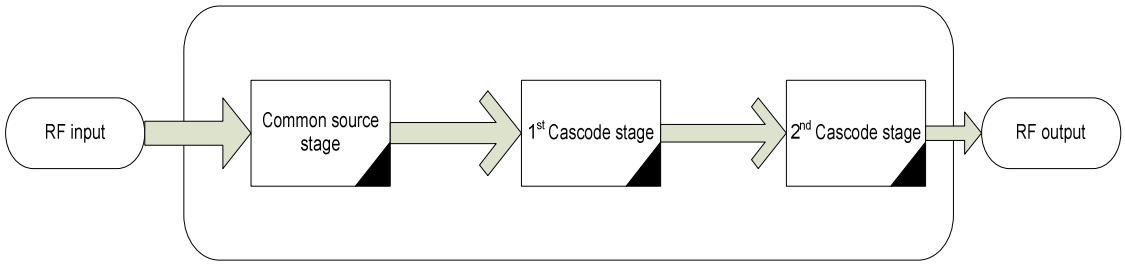

Fig 1. Block diagram of proposed Low noise amplifier

II. LNA CIRCUIT DESIGN

Circuit of low noise amplifier works on high frequency and it is designed in that way, spectrum under 6GHz is occupied by 3G and 4G services, millimetres waves that are between 30GHZ to 300GHz are fulfilling the requirements of 5G for fast operating systems and better connectivity, it should have better performance at desired frequency.

2.1 *Common source amplifier*: -

Basic common source stage is a common structure for obtaining low noise figure in circuit. It has exceptionally good sensitivity, but it has some stability problem, by addition of extra circuitry which have an inductor degeneration for desired impedance it can operate on specified frequency. This extra circuitry can also improve gain of overall circuit without affecting noise figure.

Common source circuit has better gain but poor noise performance, so here in given proposed circuit an inductive degeneration circuit is added along with common source to reduce the effect of noise in the circuit. Figure. 2 shows the circuit of common source stage of proposed circuit and total internal resistance contributed by this network is expressed in equation.1.

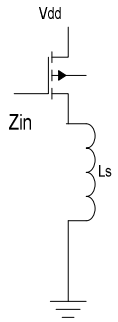

Fig.2 Common source stage with inductive degeneration circuit

$$\text{Rs } \{\text{Zin}\}=\frac{g_m L_s}{cgs} = W_T L_s \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

Despite better gain by CS topology, it has poor input impedance matching network so, here extra circuit is added to improve the input impedance matching of circuit, LC component are widely used for impedance matching. The circuit for input impedance matching from input side is as follows: -

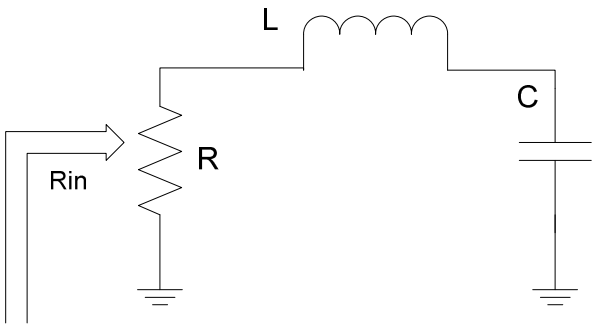

Fig.3 Input matching network of circuit

Impedance at input derived as follows: -

$$Z_{in} = j\omega L \parallel \frac{1}{j\omega C}$$

$$Z_{in} = \frac{j\omega L * \frac{1}{j\omega c}}{(j\omega L + \frac{1}{j\omega c})}$$

$$Z_{in} = \frac{j\omega L}{(-\omega^2 LC + 1)}$$

Here, ω=2Πf and f is the frequency at which circuit is operating.

The circuit for output impedance matching is required to maximize the transfer of power at output side and it also helps in reducing the input and output reflection coefficients. Output impedance matching network for proposed circuit is as follows: -

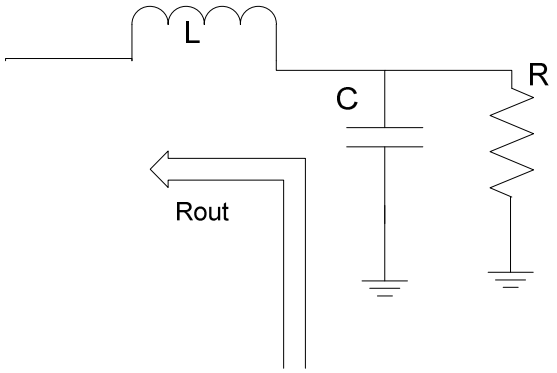

Fig.4 Output matching network of circuit

Expression of output resistance can be derived as: -

$$Z_{out} = j\omega L + \frac{1}{j\omega C}$$

$$Z_{out} = \frac{(-\omega^2 LC + 1)}{j\omega C}$$

Noise figure is one of the important parameters for low noise amplifiers and it should be kept minimum while designing of LNAs. It is highly dependent on the physical dimensions of transistor and biasing condition of circuit. LNA has an ability to amplify an output signal strength without adding extra noise. Total noise figure that is added by low noise amplifier is given as follows (equation 2): -

$$NF_{rec.} = 10log_{10}(NF_{LNA} + \frac{NF_{remaining\ module} - 1}{gain\ of LNA}) \text{ ..... (2)}$$

2.2 *Cascode stage–*

It is well known that cascode structure can highly improve the overall gain of given circuitry and it has also a particularly good reverse isolation factor.

III. CONVENTIONAL CIRCUIT

Conventional circuit has two stages, first one is common source for less noise contribution, second stage is cascode circuit used for gain enhancement. This circuit has been designed and simulated on cadence virtuoso software on 180nm technology and it has its peak value on 26GHz frequency, which is generally used in 5G applications. This circuit is compared to another low noise amplifier circuit which is designed on advanced design systems (ADS) software and this circuit has better performance in terms of gain of circuit. Here, in this circuit an extra resistive feedback has been added in the second stage for noise cancellation and better performance.

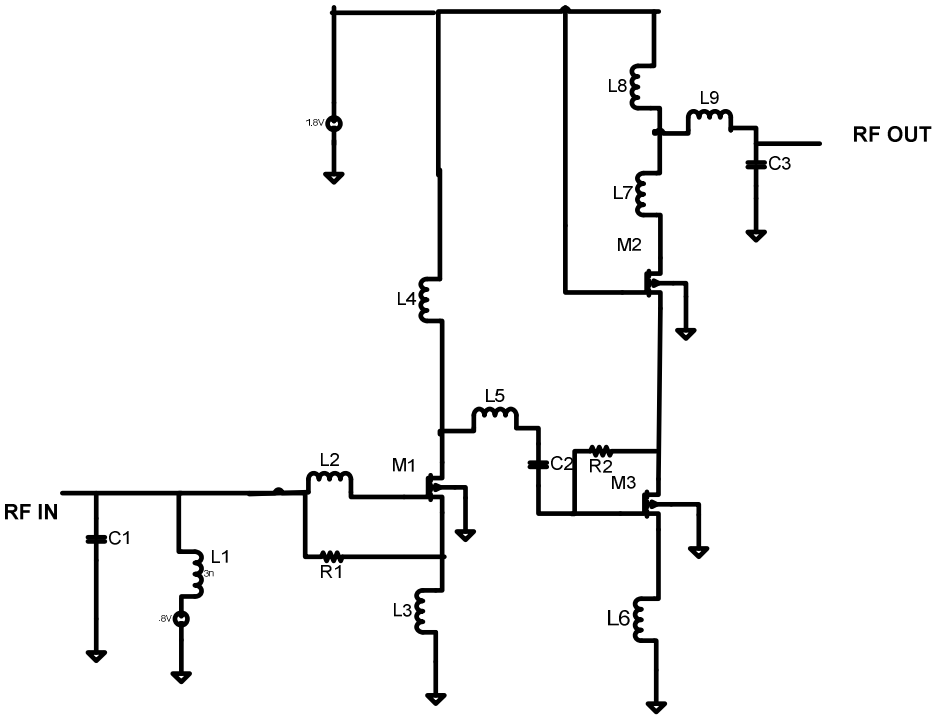

Fig.5 Conventional circuit of Low noise amplifier

IV. PROPOSED CIRCUIT

In this paper, proposed circuit is composed of three stages and it provides large gain at output without adding much noise figure at output. First stage is common source stage which is commonly used for low noise figure and high gain. Proposed circuit has LC feedback for suppressing the noise figure of circuit; here a bypass capacitor is used to bypass the noise, Second and third stage is cascode stage to improve the overall gain of circuit as the width of MOSFET affects the gain, here MOSFET with large width is used on 180nm technology. This circuit take 1.8V as supply and 0.8V to bias the initial stage of circuit. Input and output matching network are perfectly matched for the maximum transmission of gain. Dimensions of the components that are used in the proposed circuit are described in table 1: -

Table 1. Parameters of components of proposed circuit

Components	Design values
M_1	80µm/0.18µm
M_2, M_4	150µm/0.18µm
M_3, M_5	85µm/0.18µm
C_1	150fF
C_2, C_3	10pF
C_4	10fF
R_1, R_2, R_3	80KΩ
L_1	3nH
L_2	800pH
L_3	30pH
L_4	500pH
L_5	100pH
L_6	120pH
L_7	500pH
L_8	100pH
L_9	150pH
L_{10}	180pH
L_{11}	450pH

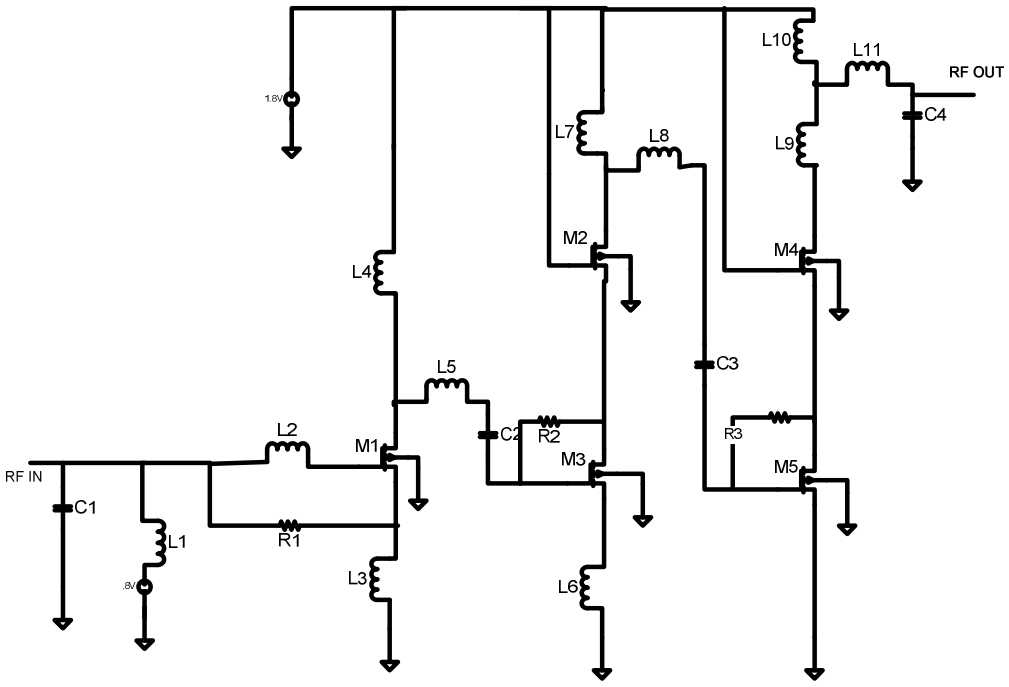

Fig.6 Proposed schematic of Low noise amplifier

V. SIMULATION RESULT**: -**

This proposed circuit is analysed on cadence software and its performance is compared with other existing low noise amplifiers. Figure.7 shows the improvement in gain(S_{21}) after adding an extra cascode circuit, but it also introduces some extra noise. Figure. 8 shows the variation of noise figure among different low noise amplifiers.

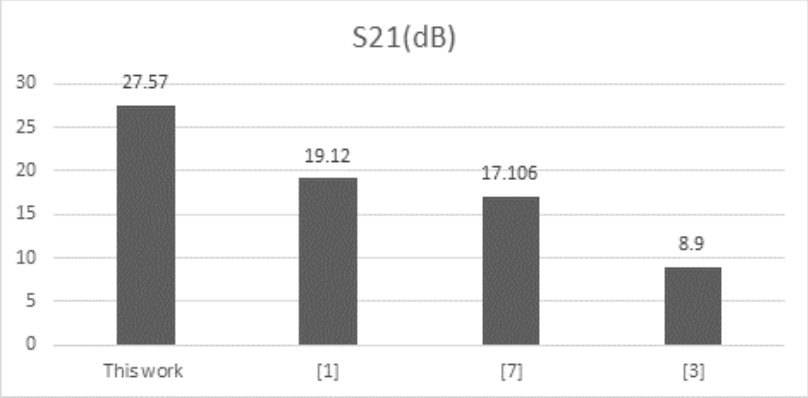

Fig.7 Analysis of gain enhancement

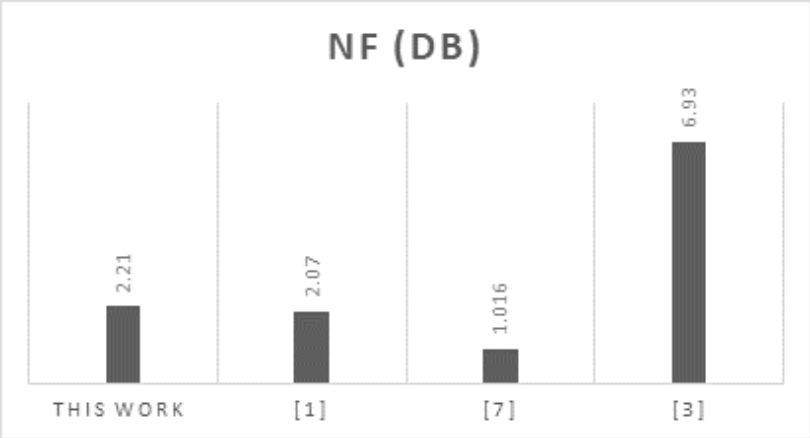

Fig.8 Variation of noise figure

The plots of all s-parameters of proposed circuit are shown in figure. 10,12,13.14. and figure.9 shows the curve of noise figure. It can be observed from the figure that there is dip at 26GHz frequency. Noise figure is minimum at 26GHz and this low noise amplifier is contributing 2.21dB noise to the system.

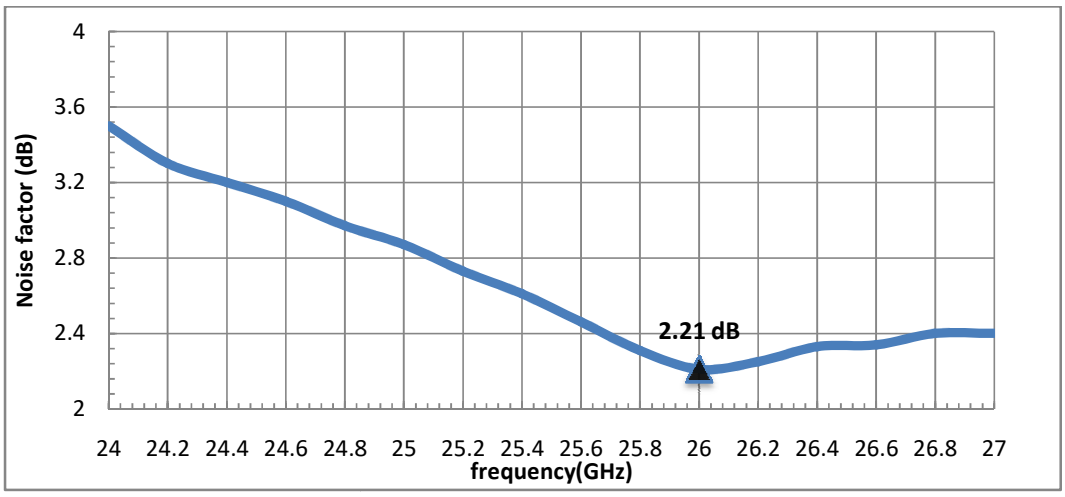

Fig.9 Curve of noise figure

S_{11} represents input reflection coefficient of circuit, here Figure 10 shows minimum input reflection at frequency 26GHz and it is -11.39dB. Output reflection coefficient of system is represented by S_{22} in Figure.11. Minimum output reflection for this proposed circuit is -9.71dB obtained at 26GHz frequency. This shows the proper impedance matching of input and output matching network, Curves of S_{11} and S_{22} as follows: -

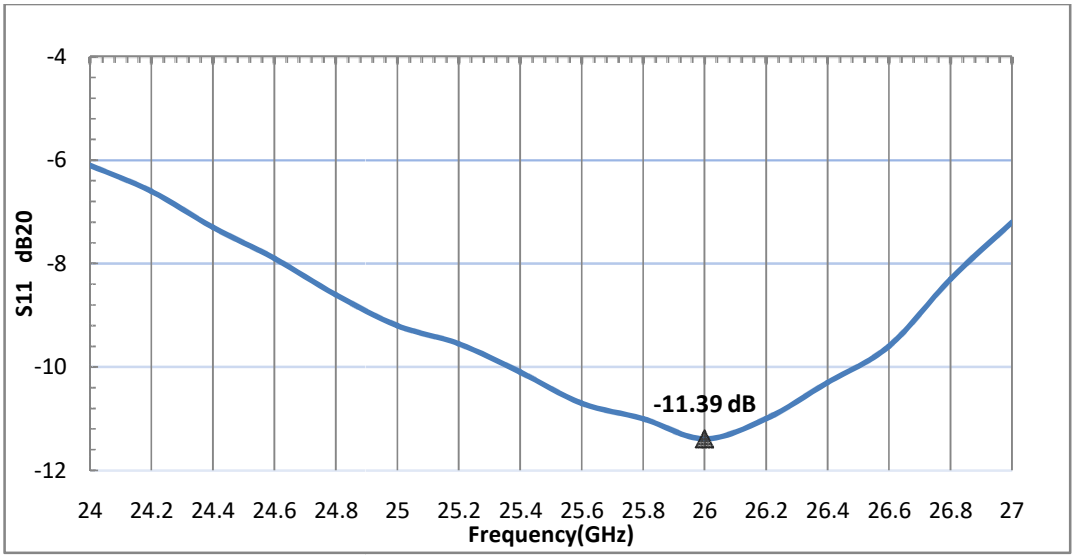

Fig.10 Curve of S_{11}

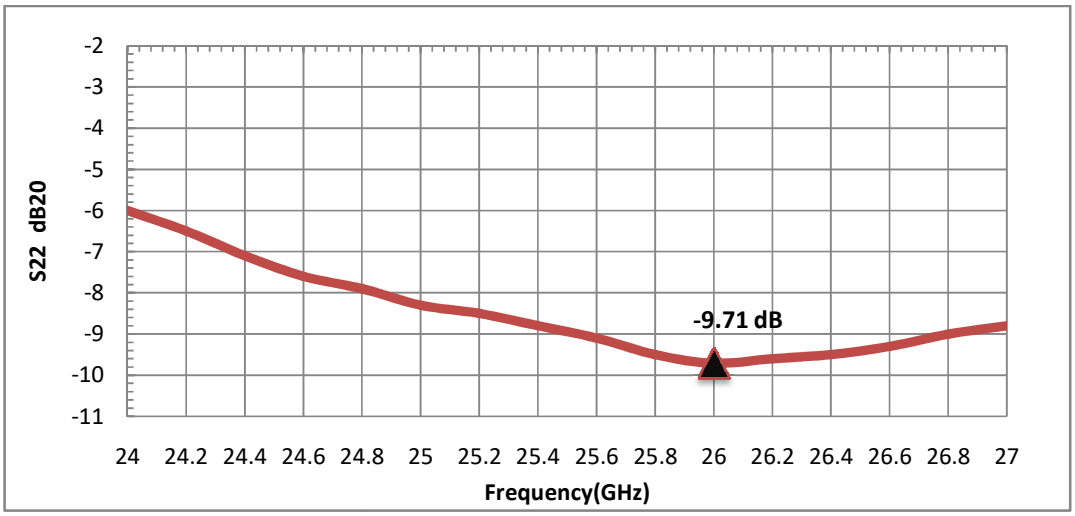

Fig.11 Curve of S_{22} parameter

Transmission coefficient of a system is represented by S_{21} and S_{12} represents the reverse transmission coefficient of system, they are shown in figure 12 and 13. These parameters gives the information about the isolation coefficient. Gain of the system is given by S_{21}, as it can be observed in figure that the system has its highest gain at 26GHz frequency and S_{12} has its peak of -83.7 dB at desired frequency, this shows a good isolation between different block of system, curves of S_{12}, S_{21} are as follows: -

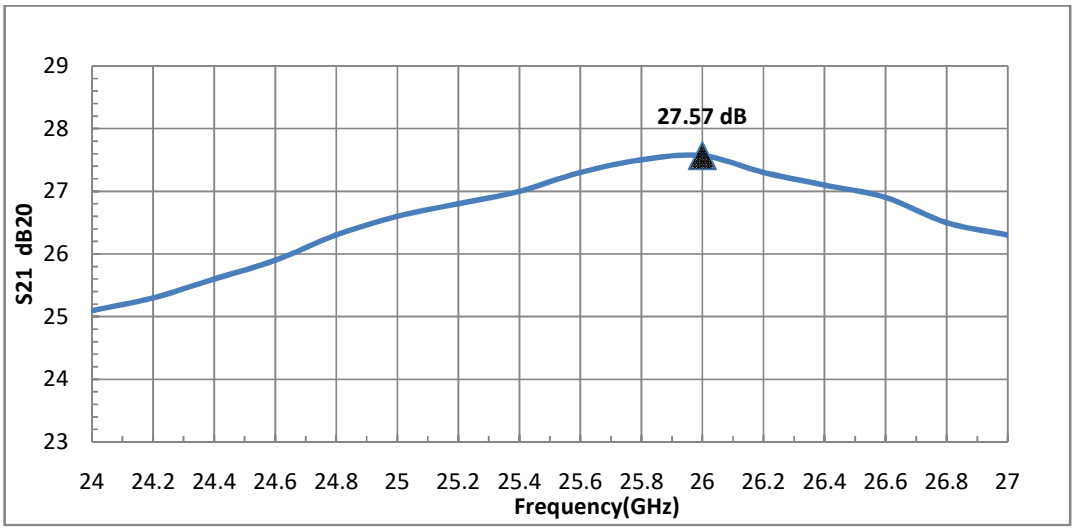

Fig.12 Curve of S_{21}

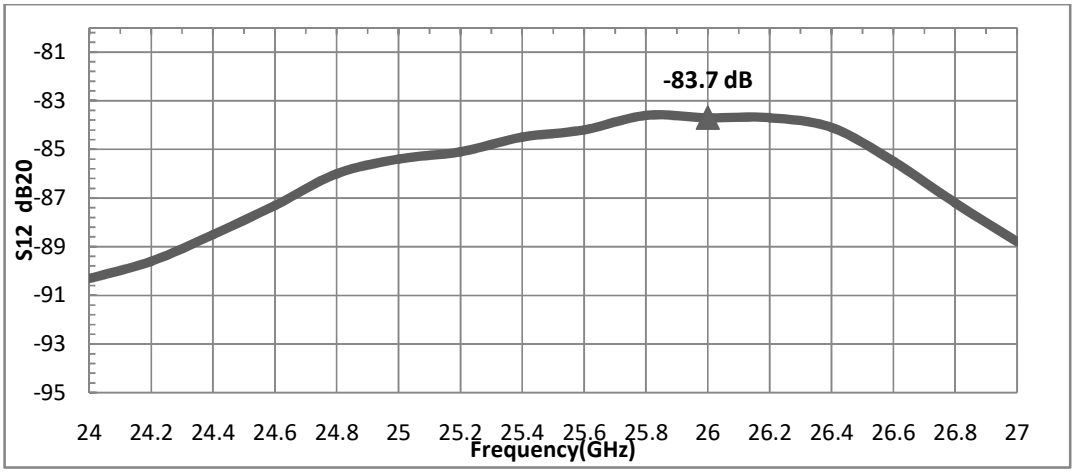

Fig. 13 Curve of S_{12} parameter

Table 2 provides the performance comparison of different types of low noise amplifiers with proposed LNA.

Table 2. Comparison study of proposed 26GHz Low noise amplifier with existing LNAs

Parameters	This work	[1]	[7]	[3]
Frequency (GHz)	26	26	26	26
Technology(nm)	180	180	180	180
Supply voltage(V)	1.8	1.8	1.8	1.8
S_{11}(dB)	-11.39	-11.683	-19.061	14
S_{12}(dB)	-83.7	-44.54	-27.365	-
S_{21}(dB)	27.57	19.12	17.106	8.9
S_{22}(dB)	-9.54	-8.431	-37.919	12
NF (dB)	2.21	2.07	1.016	6.93

VI.CONCLUSION

In this paper, using Cadence virtuoso 0.18µm CMOS technology, a 26GHz LNA has been simulated for 5G applications. This proposed circuit has provided 8% improvement in overall gain of circuit. Proposed LNA for 5G is compared with previous work in tabulated form and it has better performance than existing circuits concerning gain of the circuit. This 5G LNA is mainly targeted to be used for different wireless applications.

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