FPGA BASED PRE-EDGE DETECTIONS FOR SIMULATION

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Abstract

The proposed system is developed for time consume software based transients simulators & incorrect FPGA based digital simulators motivation at a designing into FPGA based transient error simulators as help in the designed or evaluate to the error tough methods. In this paper is example, we implement the separate circuits characterized from error simulation circuits characterization has been done at efficiently useful from standard CAD tool, As the lengthy error simulations has done as a fastly FPGA based error simulators. The Fastly FPGA platform is allowing to the delay model & errors model is a fully exercise, & the interaction among the error and circuit is to capture form best coverage's.

Keywords: FPGA based error simulators, Pre-edge methods, CORDIC processors etc.

1. Introduction

Although in this error resilient designed technique has improved into circuits reliable or reduces designed margin, it has been repeatedly complex to precise evaluation in these technique into designing time. Convention software based transient's circuits simulation uses at commercially CAD tool become slower for the additions of the transient errors effect into reached as a best coverage [1]. FPGA will be uses to accelerate errors simulation, so previous workings have been imperfect to cycle based "digitalized" simulation within uncouth delay & error model [2, 3].

2. FPGA based transient errors simulator

The propose FPGA based transient's simulators as comprises into three main part is shown as Figures 1: (1) delay profile to the data path below tests, (2) transient errors model, & (3) error resilient design has evaluate. Every one as three part is programmable, producing on versatile and generally purpose errors simulation platforms.

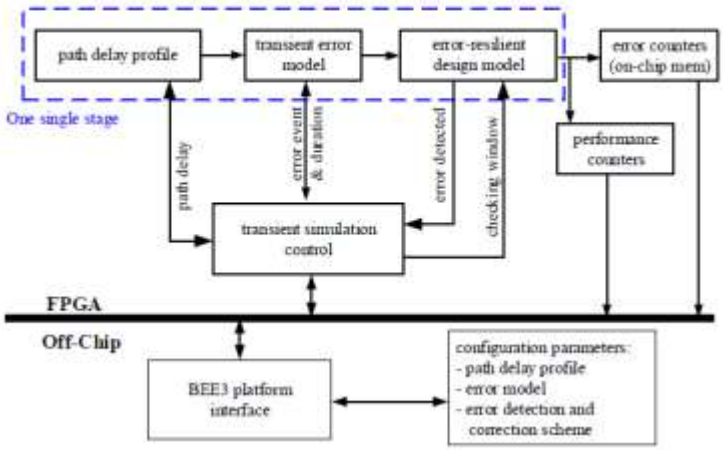


Figure 1: FPGA based transient simulator platforms. At multi stage simulations may be constructs through cascading single stage within being delay profile and model.

3. Transient error simulators

Transient simulations are frequently carry out into more finer time steps as to mimic at closed on possible the circuit continue time behavior include voltage and currents. Form error simulations, the continue monitored may be simplify in the monitor of the event, like a data propagates in the ending of the data paths, at errors upset on output nodes, etc. In the previously, “digitals” errors simulation are made to the assumption in that error event like transient fault only happen at clock cycle boundary [2]. It simplify assumption allowing in error simulation is done very fastly, therefore it is two intrinsic problem: (1) transient timing effect is neglects, example at a transient faults at a soft errors are sometime mask without introduces on the event of errors because of timing masking and (2) error resilient circuits design cannot fully capture through a cycle by cycle digital simulations, example, in the RAZOR techniques of the double sample and corrections are not simulated.

	Transient simulator (software)	Digital simulator (FPGA)	Transient simulator (FPGA)
Simulations throughput	1	> 106 [65]	> 103
Time resolutions	fine step sizes	one clock periods	sub clock periods

Table 1: Relationship between the simulators

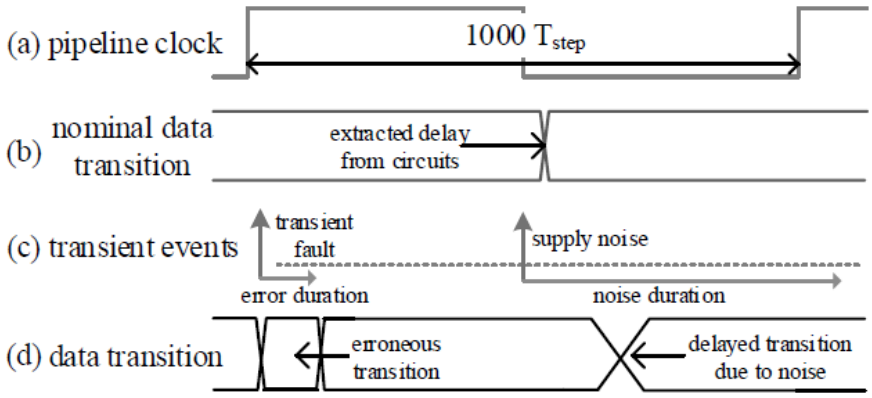


Figure 2: Timing chart to the FPGA based hardware emulations: (a) pipeline clocks,(b) extract nominal data paths delay, (c) inject transient event (error and noise), & (d) data transitions at the results with (b) and (c).

The proposes as a FPGA based transient simulations operated into finer time step & allow event into occur in these finer time step. It is used to the FPGA clock periods T_{step} at the unit's time steps. For eg, if one chosen at simulations time steps for 1ps & on clock cycle periods with 1ns, the 1ps time stepped is mapping to one T_{step} on FPGA, or the 1ns cycle periods are mapping into $1000T_{step}$. The setup permit at a simulations throughput of the $1/(1000T_{step})$. Figures 2 present on illustrations to the timing. Note on that the quality of the transient simulation depends in the time step sizes small time steps yields as more accurate result on lower simulations. At comparisons among the simulator are present into Tables 1, shows in the advantage of the FPGA based transient's simulator as provides as more accurate simulation in much high throughput than software.

3.1 Delay models and error models

The FPGA based transient's error simulators contain into three part: circuits (or data paths) delay model, error model & error resilient designed. Different on convention FPGA emulations, the data paths below tests are not direct implement on FPGA, so FPGA is use on simulator to a certain extent than prototype platforms. The data paths delay would be characterizes between circuit simulator, and the delay models are programming into FPGA form error simulations.

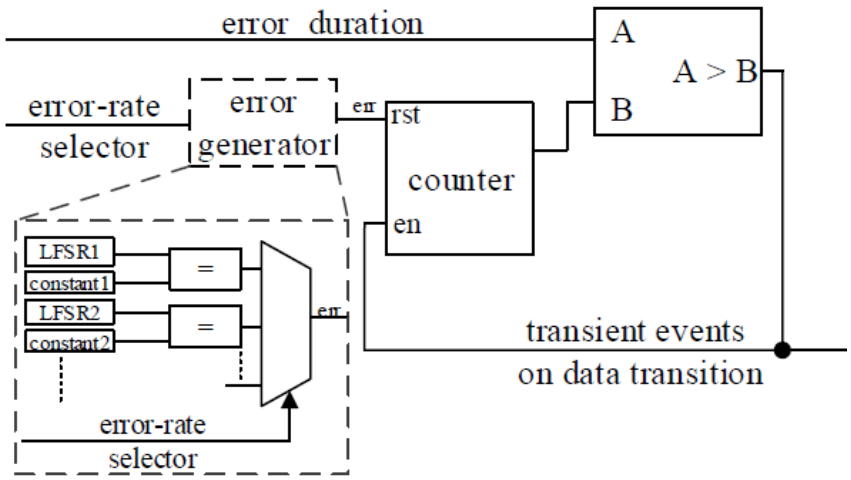
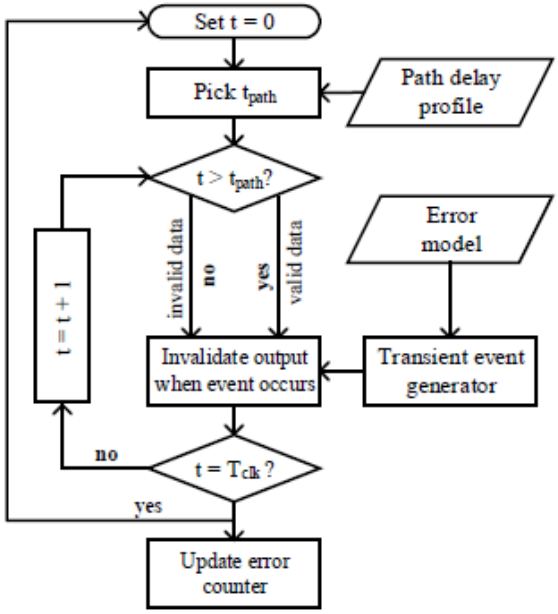


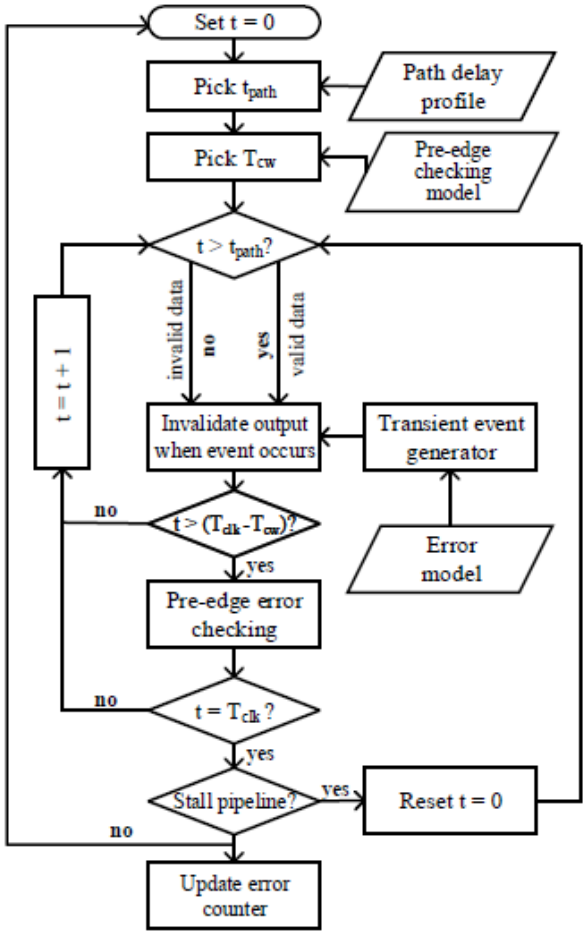
Figure 3: Transient event generators.

3. 2 Transient simulations

The transient simulators are kept on a time step counters. At the starting to the transient simulations, the time step counter is reset as 0 & the data paths delay model picked on the delay t_{path} (into unit of T_{step}) indicated in the inputs as a launch for expecting propagations delay t_{path} at illustrates into Figures 4(a). The output data's are initializes as invalid & remaining on invalid awaiting the time step counter reaching t_{path}. The transient simulations as proceed into step of the T_{step} and the time step counter increment through 1 every step. In the every simulations step, all error models decided otherwise to generate at a error base selecting errors rate. With Figure 4(a), if the transient events are generating, the outputs are invalid form the durations with the transient events. If the voltage droops are generated, t_{path} as length or short becoming as selected sinusoidally functions. The transient simulations is controller keep on tracking in the time step counter, data paths delay, error state, and make update in the output indicators. Whenever the time step counters are reached in the clock periods T_{clk}, to the controller inspect the output indicators and record on error but the output is invalidation. The transient simulations after move to the next clock periods. The time step counter reset as a 0 & a new paths delay are picked & the process continue.


Set t = 0
Pick t_{path}
Path delay profile
$t > t_{path}$?
invalid data
no
yes
valid data
Error model
t = t + 1
Invalidate output when event occurs
Transient event generator
no
$t = T_{clk}$?
yes
Update error counter

(a)


Set t = 0
Pick t_{path}
Path delay profile
Pick T_{cw}
Pre-edge checking model
$t > t_{path}$?
invalid data
no
yes
valid data
t = t + 1
Invalidate output when event occurs
Transient event generator
no
$t > (T_{clk}-T_{cw})$?
yes
Error model
Pre-edge error checking
no
$t = T_{clk}$?
yes
Stall pipeline?
yes
Reset t = 0
no
Update error counter

(b)

Figure 4: Transient simulations state (a) with the data paths delay profiles & transient error models, and (b) the state within pre-edge error detections and recovery through stalling the pipeline.

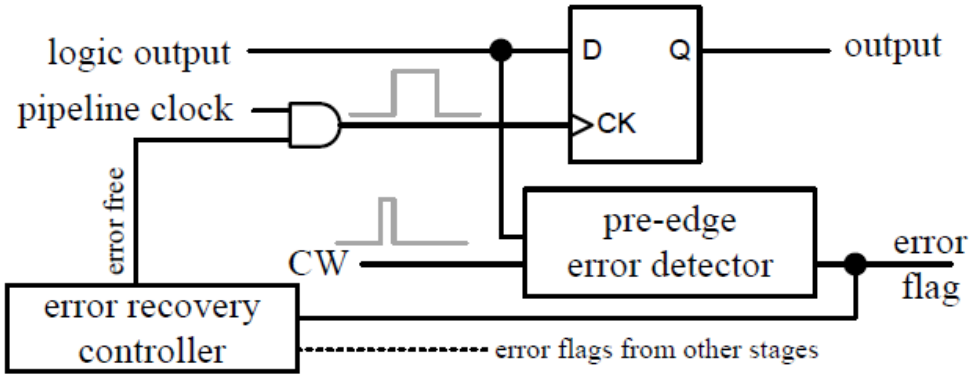


Figure 5: Pre-edge error detections & recovery between pipeline stall [4].

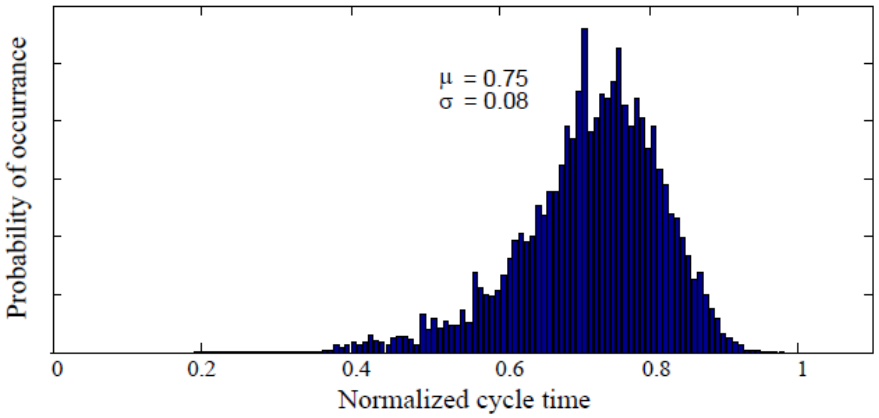


Figure 6: Simulation for delay distributions with extract CORDIC processors.

On the performances are counter to keeps as a tracks of the numbers of output produces, & as errors counter as tracking in the numbers of mistaken output jointly within the time step counters, the simulator measured in the performances and error rates.

4. Evaluations of the error adaptation design

The completely transient errors as simulators are implementing on the BEE3 platforms with multi stages pipeline. Every pipeline stages are modeled uses at a indivually data paths delay models. Soft errors, coupled in noise or voltages droop is add in the simulations. We performing experiment onto represented as data path & error model form evaluated as commonly error detections & corrections circuit technique.

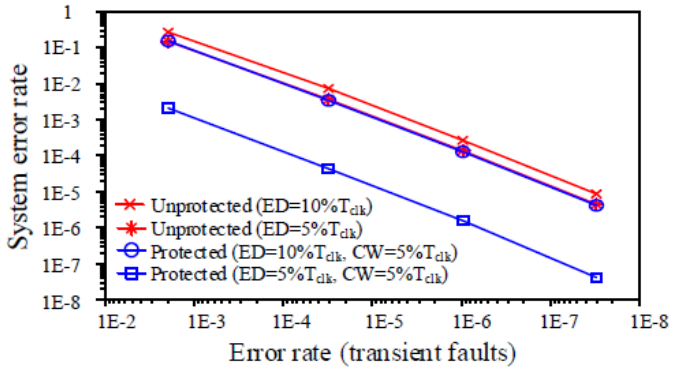


Figure 7: Reliable improvement for pre-edge errors detections and corrections (CW: checked window, ED: error durations, T_{clk}: clock periods).

4.1 Pre-edge techniques

The pre-edge error detections and corrections, as shown into Figures 5, was proposed into monitored error through the detected as glitch to the checked windows before the output is register. The pre-edge techniques are effectively as detected into slow changes as a NBTI-induce PMOS age and random transient fault. At longer check as windows *CW* provide better protections next to error to the costs of the lengthen the clock periods and degrades performances. The pre-edge error detections are accompany by a pipeline stalls as correcting the error [1].Pre-edge error detections as trigger pipeline stall to correct error, as leading to throughput degradations. Transient simulations as show in that the throughput to the CORDIC processors are mainly determine through the errors rate & the length of the *CW* , on shown in Figures 8. Lengthen of *CW* enhanced in the error protections, so as also increased.

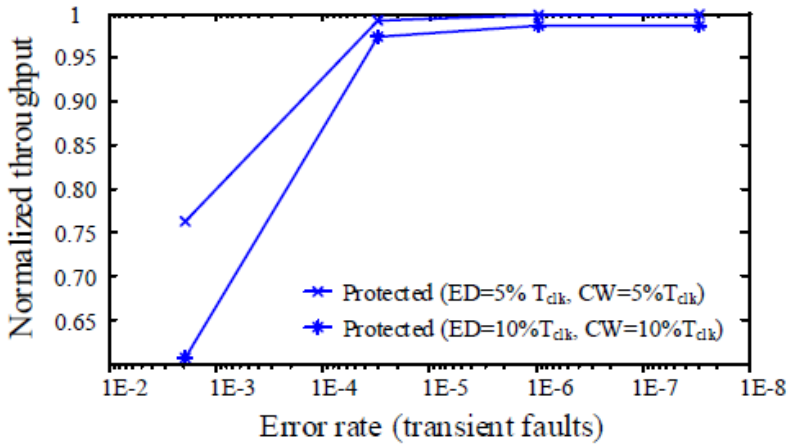


Figure 8: Effectively throughput use as pre-edge error detections and corrections (CW: checking window, ED: error durations, T_{clk}: clock periods).

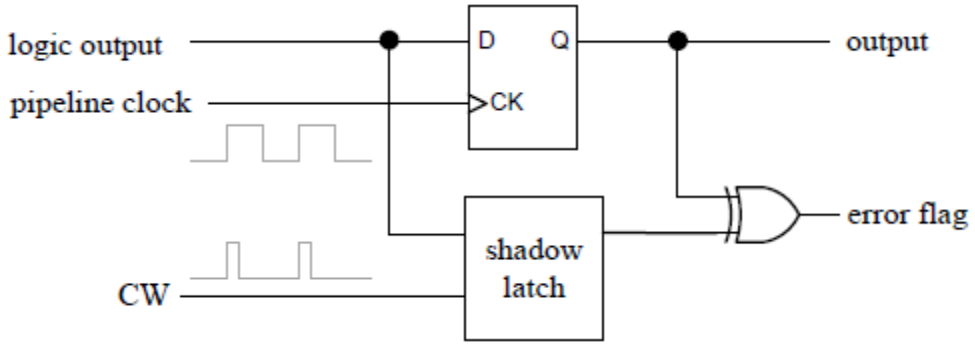


Figure 9: Post-edge errors detection circuit [5].

To the chances of the detected data transitions as the critical path and so degrade in the throughput. The trade-off among the reliable and performances as obtains with the transient simulations may be used to guide practical design.

4.2 Post-edge techniques

The post-edge error detections and corrections techniques are very popularly onto higher performances, lower power design. The post-edge techniques, is illustrates into Figure 9, detect error then the clock edges, on allow in corrections of the delay error for longer path in that exceeds in the clock cycle times [7]. The techniques are often applied into conjunction for dynamic voltages and frequencies scaling as increased in the clock frequency form high performances, or reduced in the supplying voltages form low power consumptions. We estimate the post-edge error detections and corrections on alpha processors [7] (i.e), synthesizes on 45nm CMOS technology. An application trace is obtains to the execution stages to the Alpha processor runs in the instruction into recursive Fibonacci number generations. We considered in the effect of coupling noises and voltages droop to the alpha processor.

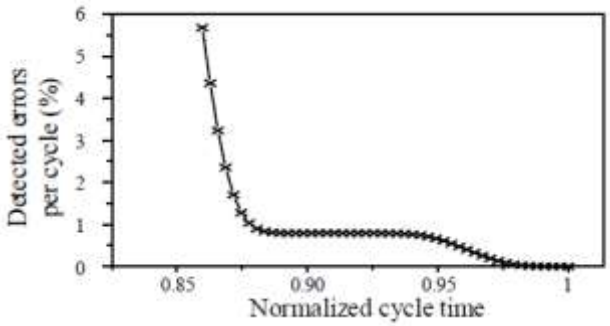


Figure 10: Post edge error detection rates.

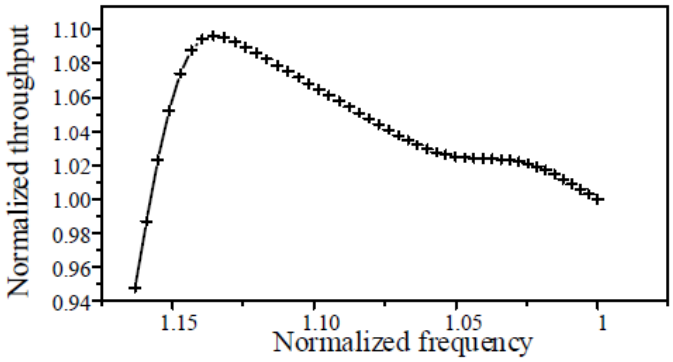


Figure 11: Effective throughput by post-edge error detections and corrections.

The alpha processors are simulation for post edge error detections. At fixing post edge *CW* is selects based to the fast path delay as avoiding into holding time issue. Dynamic frequency scaling on applies to the taking advantages in the post edge error detections and corrections. At the clock periods as decrease within increases as frequency, more error is detecting at shown in Figures 10. Error may be corrects using instructions flushing and systems nuke that is aid through the micro architectures & operating systems. Though, error corrections are usually introduced in the few cycle of the fine and the throughputs take hits. Considered at an average as five cycle of the penalty as flushes in the alpha processor pipeline & reissue the instructions, the effective throughput uses dynamic frequency scaling may be measure on Figures 11. The peak throughputs are achieved at a 1.13 time in the nominal frequency. Like a designing at explorations involves as reliable and performances may be quick obtains as using the FPGA based transient error simulators.

5. Conclusion

These chapters are present at a new efficiently and the simulation error detections method is enhanced into systems reliable next to delay & soft error. The techniques are exploited into data paths as critical among the appropriate adjust to the checking windows form high performances as minimized race condition. The error detection techniques are implementing into flexible crossing edge checking circuits in that rely onto the in-herent redundancy without resorts as a additional storage and duplications, therefore the implemented as cost is kept lower. Among duty cycling the clock signals, the checking windows may be adjusts us to provides several level of

the protections. An alternatively pre-edge circuits are also proposes as to assurance the alignment to the checking windows & the sampling edges form zero holding time. The flexible or lower cost techniques as provide into varied path coverage in the fully protects as error resilient systems. To rapid evaluated into error detections technique, on FPGA based transient's simulation form error resilient circuits and systems designed & evaluations. The common purposed on simulator consist of the configurable data paths delay model and error model is widely applicable. Error resilient circuits are designed into technique, includes as pre edge & post-edge error detections and corrections, is simulating onto platforms based synthesized CORDIC processors and the alpha processors. The simulation is lean-to light onto key design choice, like as the lengthen of the pre-edge checked windows and its impacts onto reliable and performances. The FPGA based transient simulations are complement circuits simulator and systems emulate on useful tools form resilient circuits and systems designed.

6. Reference

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