# EVALUATION OF THE CONTEXT-BASED IMAGE ACQUISITION ARCHITECTURE ON RECONFIGURABLE PLATFORM

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**Abstract**

A CBIA design of architecture is given which is based on the theory of Context- base Image Acquisition framework. The implementation and estimation as the proposed design is on the reconfigurable hardware platform of FPGA and structured-ASIC. Evaluation results show the potential of the prototype system in reducing the overall bandwidth, energy, and time, cost of the images acquisition procedure, compared with conventional method.

Keywords: CbIA, FPGA

## 1. Introduction

Based on the proposed theme of Context-base Image Acquisition, a hardware CbIA architecture is designed and implemented on custom hardware. The designing of the CbIA construction is to investigate the validity and potential of the idea in practical hardware systems of modern technology scale. The designed architecture aims to achieve a reduced cost of image acquisition (bandwidth, time, and energy consumption as is defined in the previous chapter) by the adaptive sampling and reconstruction procedures.

The design of the CbIA architecture follow the system of Context-base Image Acquisition introduce and is support at the scenario set in Section [3]. Image point sampling is core of architecture that helps to the construction to accomplish the progressive data acquisition method described [3]. A review of related image point sampling algorithms is provided in Section [4][5].The various h/w platform custom Field Programmable Gate Array is choose of the estimation proposal appropriate for relatively low design cycle and customizable structure. Design tools provided by major FPGA manufacturers such as Altera and Xilinx are well developed, offering a well supported design flow and reliable evaluation data. In the ideal situation of ASIC implementation of the proposed system, overhead cost introduced by the complication of the accessing process can be minimized. At this project, structure-Application Specific Integrated Circuit chips

among the Altera are utilize to estimate the Application Specific Integrated Circuit developing performances' reason to the easy compatibility and low design cost with FPGA design.

The CbIA construction of design is described. A prototype system makes use of basic models of natural images. It sticks to the bare bone of the proposed concept without sophisticated algorithms, to establish a practical and demonstrative model of the proposed idea. This architecture is evaluated from various aspects discussed, showing its capability of making trade-offs b/w cost metrics of image acquisition and image quality.

## 2. The Main Contribution of CbIA Architecture

1. A hardware architecture of the proposed CbIA framework is designed and implemented on Field Programmable Gate Array and structure-Application Specific Integrated Circuit device.

2. A set of the evaluations are conducted on the implemented architecture, demonstrating the potential of to the proposed organization in reduce the cost (bandwidth, time & power consumptions) of images acquisition method in practical hardware environment.

## 3. Evaluation as the Design CbIA Architecture

The designing of CbIA architecture is evaluated on reconfigurable hardware platform for its impact on the general cost as image acquisitions method. The evaluation in this section takes into consideration the cost of running mutually the source memory & compute engines.

The CbIA architecture was synthesized and routed and placed on Stratix Hardcopy IV structure ASIC and IV FPGA. The SDRAM(source memory) reply & the rest at the Synchronous Dynamic Random Access Memory accessing interfaced is mutually simulating by Modelsims test bench instead of being implemented. The generated SDRAM access address is approved to Synchronous Dynamic Random Access Memory power mode is designing through Rambus &HP, at this rotate report the consequent Synchronous Dynamic Random Access Memory energy using as the i/p access example. Again different 1GbDDR3 are simulating through the power model as of Rambus[1] is

target SDRAM, and the test is furthermore carry out from two slighter size Synchronous Dynamic Random Access Memory memories model with the CACTI tool considered by HP[2]. The SDRAMs simulated by CACTI equipment and Rambus model CACTI models

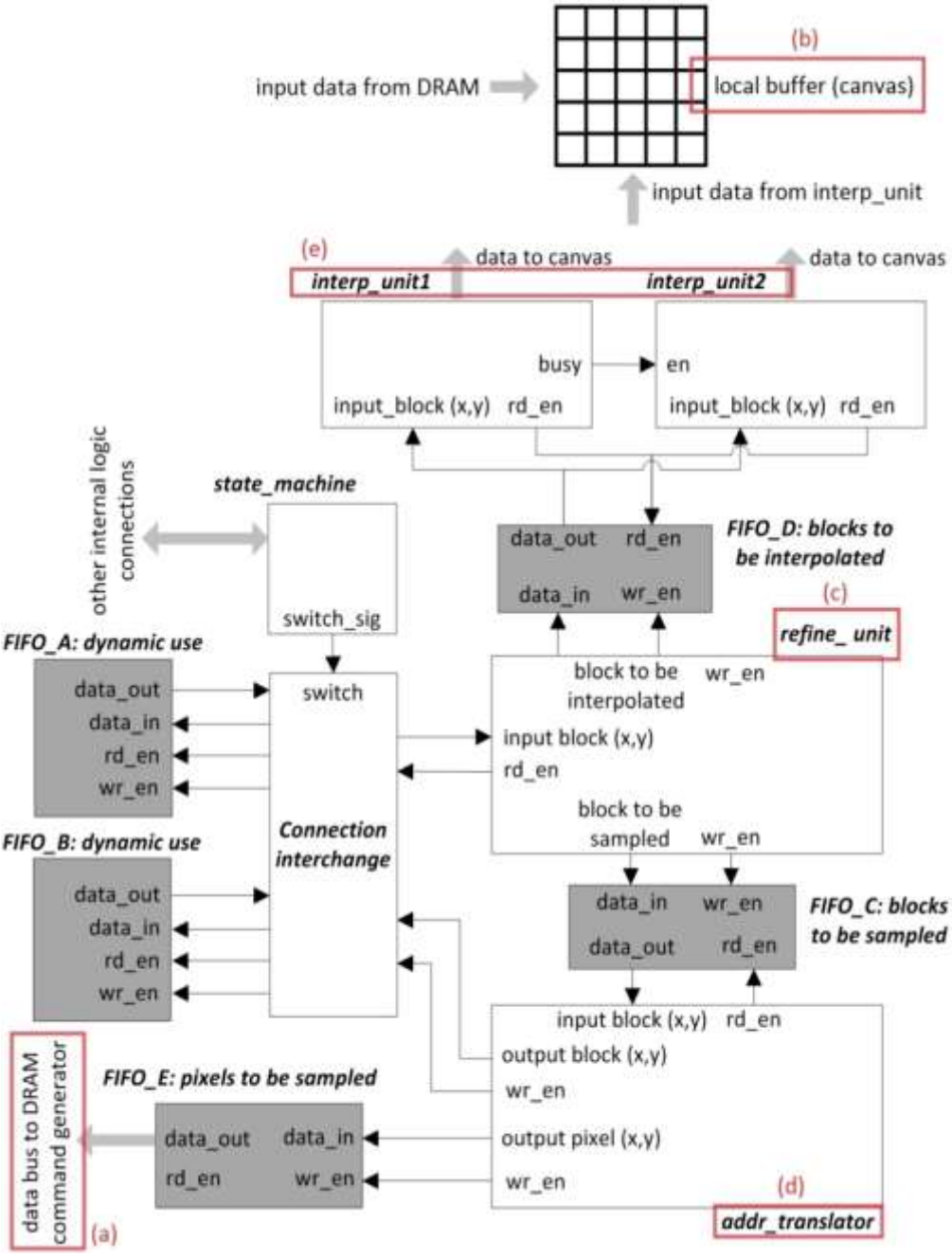


Figure .1: The formation as the proposed CbIA architecture. (a) The projected designing generate pixels address since the DRAM interfaced; (b) a limited canvas buffer stores sampling pixels also interpolating pixels; (c) the purify units check precedence scores of every block; (d) the address translator generate sampling address

but a blocks are to be delicate; (e) an array is interp unit interpolates the misplaced pixels with blocks that do not require additional sampling/ refinement.

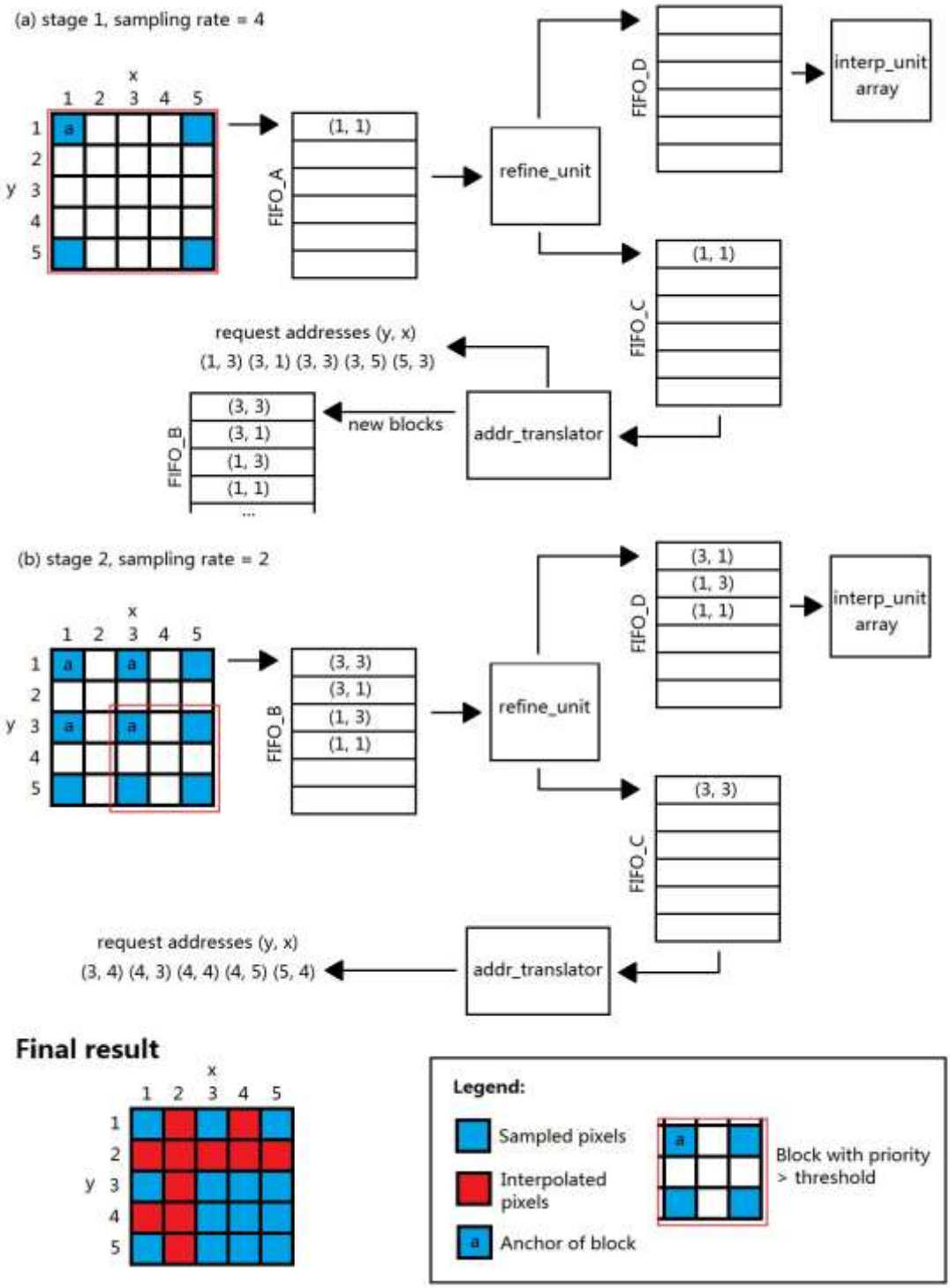


Figure .2: Example of system working controlling. a 55 nm & 45 nm technologies correspondingly, even as together with 8 bit I/O and had a burst span of 8. Block map image substance is utilized in to subsequent test from the most admired store plan use in image methodology h/w systems.

The synthesized architecture perform restoration and sampling of to the selected benchmarks images these are: “Barbara”, “lena”, and “boat”. All are of sizes 527x527 and convert to grayscale image by each pixel represent by a 8-bit value. The framework works at non-overlapping macro blocks of size 17x17 from the aim image. From every test, the construction progress the threshold as 1800 (bad worth) to 150 (good worth), regularly increase the no of sample.

from the set of opinion, the projected CbIA structure is thought to assumed at the equal frequency because the memory facts bus, i.e. it had the potential to randomly get admission to a single 8-bit pixels among the memory with out pre-fetching -analyzing successive pixels. but, as the baselines presentation (the conventional photo acquisitions technique) the goal images area is study at the nearby buffer to burst length with burst mode of eight. The assessment provides here is a decrease sure performs as the proposed CbIA structure.

In the following sections, the proposed architecture is compared with conservative address generators in Synchronous Dynamic Random Access Memory right to use interface, to the variation in image acquisitions time & overall power utilization in the acquisition method. It is worth noting that the cost in bandwidth is covered and therefore is not repeated at this section. Besides the evaluation of the performance of the CbIA structure, another evaluation is provided on the impact to the projected CbIA process to a image compression applications. at last the mapping since FPGA performance to ASIC implementation is discuss.

| | Combinational ALUTs | Logic registers | Block RAM | | DSP block 18-bit elements |
|---|---|---|---|---|---|
| | | | bits | # of M9K | |
| refine unit | 114 | 110 | 0 | 0 | 0 |
| interp unit (x3) | 895 | 574 | 0 | 0 | 41 |
| addr translator | 87 | 77 | 0 | 0 | 0 |
| FIFOs | 879 | 471 | 1574 | 9 | 0 |
| Control | 91 | 21 | 0 | 0 | 0 |
| Total | 1171 | 1253 | 1574 | 11 | 41 |
| Total (%) | 0.59% | | 0.006% | 0.9% | 4.25% |

Table 1: Hardware resources utilize of to the proposing system, on Stratix IV. The % resource use at the last row show the percentage of total resources as the considering type utilized from the devices.

| | H cells | Block RAM bits | DSP block 18-bit elements |
|---|---|---|---|
| total | 49693(0.55%) | 1574 | 41 |

Table 2: H/w resource utilize as the proposing system, on Hardcopy IV. A total of 0.55% of to the total HCell source on device is used.

## 4. Evaluation as the Proposed Architecture on Reconfigurable Platforms

### 4.1. Hardware resources utilize

The predictable addressing generator at DRAM interfacing frequently acts for easy counter through minimum developing cost the hardware resources need to the develop this is omitted in to this estimation. Table 1 report the add cost of hardware resources as developing the prototype system on Stratix-IV Field Programmable Gate Array. Table show a important proportion in the hardware resources, include all the blocks RAM bits & the majority as the ALUTS/registers, are utilized to maintained the intermediate data structures. The array of inter p units too use a key proportions of ALUTs & registers in they are the major computational concentrated parts at the system. Table 2 report the add cost of h/w resources as implement the prototypes system on Hardcopys IV architecture-ASIC.

### 4.2. Acquisitions time

The estimated maximum frequency of the prototypes system is given in Table 3.

| | Model ID | fmax at slow 900mV 85C | fmax at fast 900mV 0C |
|---|---|---|---|
| Stratix IV | EP4SGX530KH40C2 | 280 MHz | 412 MHz |
| Hardcopy IV | HC4GX35FF1517 | 357 MHz | 621 MHz |

Table 3: Reporte max frequencies as the design.

The Synchronous Dynamic Random Access Memory accessing time ( clock cycles) also the total image acquisitions time spend include interpolations are report. This evaluation test assume that a prototypes system works under a complete random access situations, i.e. as a every address providing with the prototypes system, SDRAM proceeds only to the pixel value on that address. The orientation lines at the plots shows the image acquisitions time need with conventional image accessed method, distribute to the same clock cycles.

The possible PSNRs differs by test theme. The image "barbara" had extra difficult local structure another 2 images & therefore A PSNR in the modernization is comparatively low, even when a similar important score threshold is met. In common due to the reduce no of sample pixels, the proposing system have a much lower SDRAM occupy time (black lines) than the conventional accessing process (blue reference lines). This outcome at a greatly reduce bandwidth need of SDRAM and when need, it frees the Synchronous Dynamic Random AM early scheduled to be access with another voltage processing units as a big system. From the other hand, a important amount as a time is spend on interpolating to the image. however, A total image acquisitions time reducing in most cases on this test. at this exacting test three interp units are utilized, but more of this unit may be adding to accelerates the method in the expenditure of extra hardware resources. This is for the reason that blocks require interpolation are recorded in F IF O D & the interpolations task may be completing with multiples interp unit in equivalent.

Referring to the discussion at the design CbIA structure demonstrate that the projected framework is capables as reduce the whole image acquisitions time by employing on-chip computational resource to compensate to the choosy &loss sample method. The time cost overhead to calculation, includes that to scheming the sampling method& for interpolation, is mitigate with the advance calculation capacity as the computing engines also through design process like as parallelism of the interpolation process.

**Conclusion**

By decrease the no of times of memory accessing, a overall cost of image acquisition process can be reduced at a cost of lowered image quality in a practical hardware environment. A suitable progressive sampling algorithm/mechanism such as the proposed Adaptive Re- fine algorithm allows the CbIA architecture to dynamically adjust to the available band- width,

time, and energy resources. The CbIA architecture always refines the sampling pattern in a way that each memory access brings in a pixel considered by the sampling procedure to be most statistically significant.

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