Design of Low-Cost 3-Stage Low Noise Amplifier using Multistage Cascade and Self-Bias Method for LTE System

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Abstract—This study aims to design and develop a low-cost Low Noise Amplifier (LNA) for the LTE FDD system for LTE band 3 (DCS), which frequency is 1805 – 1880 MHz. The characteristic of the transistor that used in this study is a high gain, low noise, with a 3-stage cascade configuration to produce high gain and improve stability. The simulation results show that LNA has reached all the expected specification at the frequency of 1805 – 1880 MHz which are gain, input return loss, output return loss, noise figure, VSWR input, and VSWR output are 33.39 dB, -42.85 dB, -41.38 dB, 0.48 dB, 1.01 and 1.02, respectively. The measurement results show that at center frequency LNA obtained value of gain, input return loss, output return loss, VSWR input, and VSWR output as much as 19.72 dB, -6.78 dB, -6.99 dB, 2.69, and 2.62, respectively.

Keyword – LNA, LTE, FDD, Self-Bias, Cascade

I. INTRODUCTION

LTE technology theoretically offers downlink speeds of up to 300 Mbps and uplink 75 Mbps. LTE uses Orthogonal Frequency Division Multiplexing (OFDM) which transmits data through many radio spectrum operators, each with a width of 180 kHz. The transmission is by dividing the data stream into many slower streams that are transmitted simultaneously. By using OFDM minimize the possibility of multipath effects. To increase the overall transmission speed, the transmission channel used by LTE is enlarged by increasing the quantity of radio spectrum operators without changing the radio spectrum channel parameters themselves. LTE must be able to adapt according to the amount of available bandwidth.

In addition to the increasing number of service users, environmental factors are also a constraint on the telecommunications system. Environmental factors can cause losses that make the power emitted to the receiver

weakened so that the signal sent to the receiving device is not optimal. Therefore the system needs enhancements to strengthen the weak signal received on an antenna. The device is called the Low Noise Amplifier (LNA).

Some studies regarding LNA has already been published. In [1], the study presents a low power and wideband LNA. It uses modified derivative superposition (MDS) technology which is adopted to improve the linearity of this stage. The frequency used is 700 MHz to 1 GHz. In [2] also study to model an LNA for base station receiver. It uses GaN HEMT to improve gain. It uses the Advanced Design System (ADS) to model the LNA. In [3], [4], and [5], they try to design a high power gain and power consumption of LNA. In [3] uses a 1 – 7 GHz frequency to support many standards of wireless devices and applications, such as GSM, UMTS, WiMAX, LTE, and WLAN. The LNA consumes 24 mW power at 1.2V supply voltage. In [4] and [5], the study regarding power consumption of LNA. It is based on the sensitivity requirement of the LTE receiver. This paper discusses designing the LNA for LTE application which works in LTE band 3 (DCS). This study uses a multistage cascade and self-bias method to produce high gain and improve the stability.

II. LNA DESIGN PARAMETERS AND METHOD

LNA is a sub-system that is placed in the front end of the receiver, close to the receiving antenna. This sub-system is needed in the receiver system because the signal received by the antenna was attenuated so it needs to be strengthened before entering the down-conversion stage and baseband operation. Therefore, to get a quality signal, the LNA must have a high gain value. LNA as one of the sub-systems in the receiving system needs to be designed with a small value of noise figure (NF) so that the contribution of noise added to the amplified signal is not large or as minimal as possible [6]. The diagram block of LNA can be seen in Fig. 1.

A. LNA Parameters

LNA has many parameters that decide its performance. The parameters are gain, noise figure, return loss (input and output), VSWR, and stability.

Gain is the ratio between the system output signal to the system input signal. The gain in LNA is denoted by S21 where port 1 is input while port 2 is output. The gain of an LNA must be high and usually the standard value of more than 10 dB. This corresponds to the LNA function, which is to amplify the received signal. According to Sayre [6], noise is divided into two types, namely circuit generated and externally generated. Externally generated noise comes from outside energy, both arising from objects in the vicinity causing electromagnetic fields. While circuit generated noise comes from the internal system which can be defined as noise caused by the random movement of electron components due to heat energy (white noise) and random movement of electrons at junction semiconductor or transistor (shot noise).

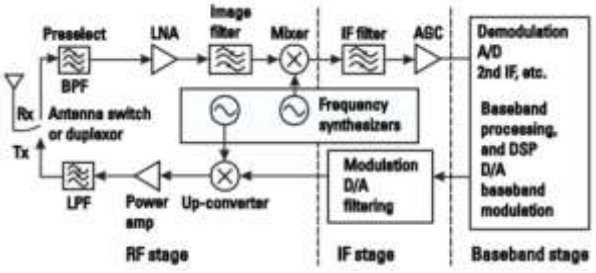

Fig. 1. Diagram block of LNA [6]

Return loss is defined as the ratio between the amplitude of the reflected wave and the amplitude of the transmitted wave. Return loss can occur due to discontinuity between the transmission line and input impedance so that not all power is radiated but some is reflected. Return loss can be explained by the two-port network as shown in Fig. 2.

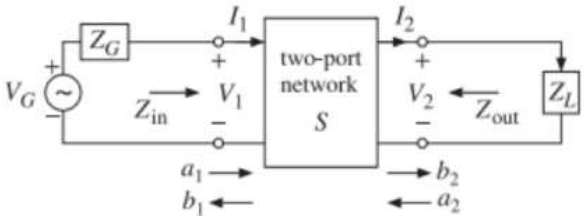

Fig. 2. Two port network [7]

The reflection coefficient on port 1 (input) is written in equation (1) where the value of input return loss, S_{11}, in dB is shown in equation (2). The reflection coefficient on port 2 (output) is written in equation (3) where the value of output return loss, S_{22}, in dB is shown in equation (4). Voltage Standing Wave Ratio (VSWR) is a ratio between the maximum standing wave amplitude ($Vmax$) and the minimum ($Vmin$). The emergence of this standing wave is caused by an incompatibility in the transmission line so that there is a dissipated power in the form of heat. Unconditionally stable conditions are indicated by a Rollett Stability Factor. If the value of K> 1, it is said to be an unconditionally stable circuit. The K value can be known from the S value of the parameter given by equation (5) [8]. LNA is said to be unconditionally stable if K> 1 and Δ <1.

$$\Gamma_{in} = \frac{Z_{in}-Z_0}{Z_{in}+Z_0} \tag{1}$$

$$S_{11}(\text{dB}) = 20\log_{10}|\Gamma_{in}| \tag{2}$$

$$\Gamma_{out} = \frac{Z_{out}-Z_0}{Z_{out}+Z_0} \tag{3}$$

$$S_{11}(\text{dB}) = 20\log_{10}|\Gamma_{out}| \tag{4}$$

$$\text{K} = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}||S_{21}|} \tag{5}$$

$$\Delta = S_{11}.S_{22} - S_{12}S_{21}$$

B. Self-bias Method

Fig. 3 shows the self-bias configuration, which is the most commonly used way to decorate JFET. Drain current flows through RD and RS, which results in the source-voltage voltage shown in equation (6) and the voltage across the source resistance shown by equation (7). Because the gate current is small so IG can be ignored and RG estimated 1 Megaohm [9].

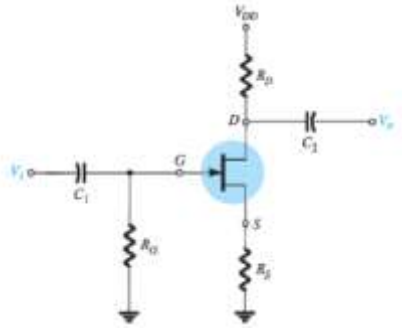

Fig. 3. Self-bias configuration

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \tag{6}$$

$$V_s = I_D.R_S \tag{7}$$

The gate terminal has a dc ground voltage, so $V_G \cong 0$. Therefore the potential difference between gate and source is shown by equation (8).

$$V_{GS} = V_G - V_S = 0 - I_D.R_S$$

$$V_{GS} = -I_D.R_S \tag{8}$$

C. Scattering Parameter

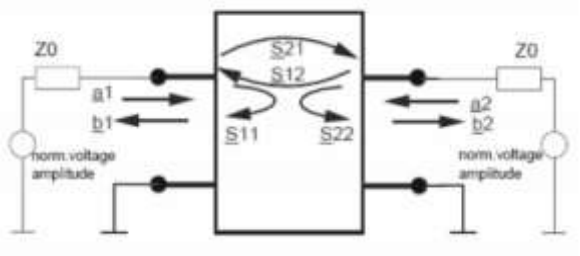

Fig. 4. Two port network for scattering parameter explain

The mathematical equation for the circuit on the two-port network is shown in Fig. 4 is explained in equation (9), where a_n represents the normalization of incoming voltage entering the two-port circuit, while b_n is normalized reflection voltage from the two-port circuit. The matrix form of the scattering parameter is shown by equation (10) [10]. The values of each scattering parameter scattering S_{11}, S_{12}, S_{21} and S_{22} are shown in equation (11), (12), (13) and (14), respectively, where, S_{11} is the input reflection coefficient, S_{12} is the reverse voltage gain (feedback), S_{21} is the forward voltage gain and S_{22} is the output reflection coefficient.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{9}$$

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{10}$$

$$S_{11} = \frac{b_1}{a_1} \text{ with } a_2 = 0 \tag{11}$$

$$S_{12} = \frac{b_1}{a_2} \text{ with } a_1 = 0 \tag{12}$$

$$S_{21} = \frac{b_2}{a_1} \text{ with } a_2 = 0 \tag{13}$$

$$S_{22} = \frac{b_2}{a_2} \text{ with } a_1 = 0 \tag{14}$$

D. LNA Design Specification

To get good results according to the needs of the LNA design, designers usually combine two or more transistors. These configurations include cascode and cascade. The advantage of a cascode configuration is that it has high isolation between the input and output ports so that the input and matching impedance parts can be done separately. In contrast to the cascode, in the cascade configuration, the output of the first stage is connected to the second level input so that the signal experiences a gain of two times or in other words, the gain is very high because it follows the number of stages used [11].

The purpose of this research is to be able to design, make and test LNA at a frequency range of 1.805 – 1.880 GHz with a 3-level cascade method with self-bias refraction, with test criteria can be seen in Table I. The transistor used in this research is the production of Avago Technologies with type ATF-34143. The main specifications can be seen in Table II.

Table I. LNA Specification

Parameter	Specification
Frequency	1.805 – 1.880 GHz
Gain	>18 dB
Noise Figure	<1 dB
Input return loss	<-10 dB
Output return loss	<-10 dB
VSWR input and output	<2
Stability factor	>1
Input and output impedance	≈50Ω

Table II. ATF-34143 Specification

Parameter	Specification
Transistor Type	PHEMT
Frequency range	450 MHz – 1 GHz
Noise figure	<1 dB
Gain	>15 dB
Temperature	-65 – 160 C
Idss max	145 mA

From Table II it can be seen that all LNA specifications can be fulfilled by the transistor used. ATF-34143 transistor is a type of PHEMT (Pseudomorphic High Electron Mobility Transistor) which is a development of HEMT and is one of the categories or families of FET (Field Effect Transistor). The performance of HEMT shows a low noise figure and high gain up to a frequency of 70 GHz, so it is very suitable for LNA [12].

Table III. ATF-34143 Electrical specification

ATF-34143 Electrical Specifications

T_A = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameters and Test Conditions			Units	Min.	Typ.[1]	Max.
I_{DSS}[2]	Saturated Drain Current		V_{DS} = 1.5 V, V_{GS} = 0 V	mA	90	118	145
V_P[2]	Pinchoff Voltage		V_{DS} = 1.5 V, I_{DS} = 10% of I_{DSS}	V	-0.65	-0.5	-0.35
I_D	Quiescent Bias Current		V_{GS} = -0.34 V, V_{DS} = 4 V	mA	—	60	—
g_m[2]	Transconductance		V_{DS} = 1.5 V, g_m = I_{dss}/V_p	mmho	180	230	—
I_{GSO}	Gate to Drain Leakage Current		V_{GD} = 5 V	µA			500
I_{gss}	Gate Leakage Current		V_{GS} = V_{DS} = -4 V	µA	—	30	500
NF	Noise Figure	f = 2 GHz	V_{DS} = 4 V, I_{DS} = 60 mA	dB		0.5	0.8
			V_{DS} = 4 V, I_{DS} = 30 mA			0.5	
		f = 900 MHz	V_{DS} = 4 V, I_{DS} = 60 mA	dB		0.4	
G_a	Associated Gain	f = 2 GHz	V_{DS} = 4 V, I_{DS} = 60 mA	dB	16	17.5	19
			V_{DS} = 4 V, I_{DS} = 30 mA			17	
		f = 900 MHz	V_{DS} = 4 V, I_{DS} = 60 mA	dB		21.5	
OIP3	Output 3rd Order Intercept Point[3]	f = 2 GHz +5 dBm P_{out}/Tone	V_{DS} = 4 V, I_{DS} = 60 mA	dBm	29	31.5	
			V_{DS} = 4 V, I_{DS} = 30 mA			30	
		f = 900 MHz +5 dBm P_{out}/Tone	V_{DS} = 4 V, I_{DS} = 60 mA	dBm		31	
P_{1dB}	1 dB Compressed Intercept Point[3]	f = 2 GHz	V_{DS} = 4 V, I_{DS} = 60 mA	dBm		20	
			V_{DS} = 4 V, I_{DS} = 30 mA			19	
		f = 900 MHz	V_{DS} = 4 V, I_{DS} = 60 mA	dBm		18.5	

After determining the type of transistor corresponds to the LNA parameters to be designed, the next step is to provide a bias for the transistor to be able to work at its working point. There are several types of biasing that can be used, including fixed bias, voltage divider, and self-bias. This study uses self-bias because it is more efficient (requires one dc supply) and the most commonly used for FET bias. For transistors to work properly, they must be designed according to their working points. The work point is a fixed point in a characteristic curve of a transistor, usually called a quiescent point. In refracting this transistor, the researchers determine the values of VDS (4V), Id (60mA), and VGS (-0.34) from the datasheet that shown in Table III as a reference to calculate the resistor value used in the bias circuit. Whereas the L and C blocking values are adjusted to the best simulation results.

In the cascode configuration, the drain terminal of transistor 1 is connected to the source terminal of transistor 2, so it is known as the Common Source Common Gate. Whereas in the cascade configuration, the output of the first stage is connected to the second level input so that the signal has a gain of 2 times or in other words, the gain is very high

because it follows the number of stages used. Another advantage of the cascade is noise and better stability compared to cascode stacking. Therefore, researchers used a cascade configuration in the design of LNA.

As for determining the number of stages (levels) is following the needs of the LNA to be designed. In this study, the LNA parameters for gain is more than 18 dB and the noise figure is less than 1 dB. Therefore, the researchers made an LNA design with a 3-level stacked cascade configuration, because it was feared that there was a mismatch or shift when measuring LNA. Fig. 5 shows a 3-level stacking LNA design using ADS.

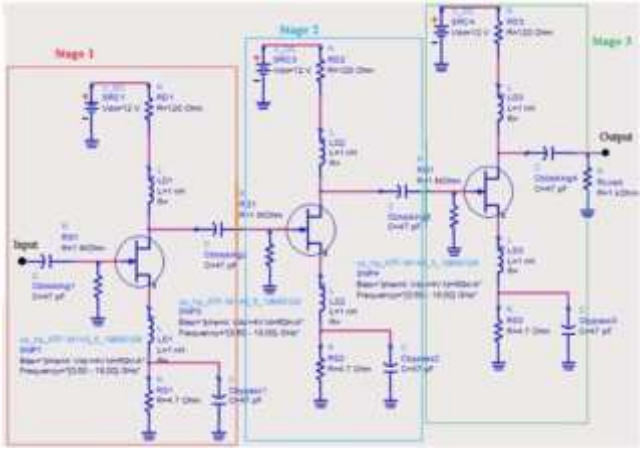

Fig. 5. LNA design with 3-stage cascade using ADS

There are several methods used to create matching channels on LNA, including microstrip channels, L-network, T-network, and p (phi) -network. In this study, researchers used the concept of L-network, like shown in Fig.6 because this matching impedance is the most commonly used and simplest way to assemble it, with just only L (inductor) and C (capacitors).

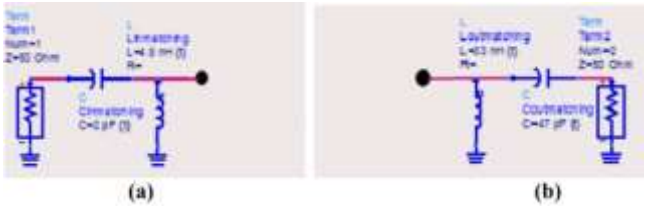

Fig. 6. L-network design for input impedance (a) and output impedance (b)

III. DESIGN AND FABRICATION

To realize an LNA, an LNA design is required first. In this design, a low noise amplifier will be designed using a 3-level cascade configuration. The aim is to increase the value of the gain, decrease the value of the noise figure, and increase the stability of the LNA circuit. In the design, refraction used for this LNA is self-bias refraction. Before fabrication, LNA layouts are made, that can be seen in Fig. 7

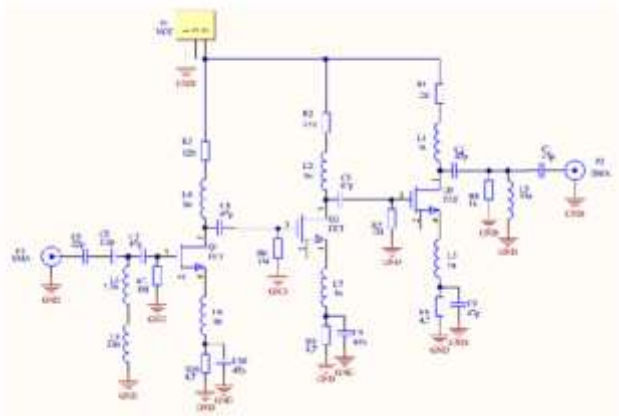

Fig. 7. LNA design layout

From the design and calculation above, the simulation results obtained can be seen in Fig. 8 and the C and L values are shown in the Table. IV.

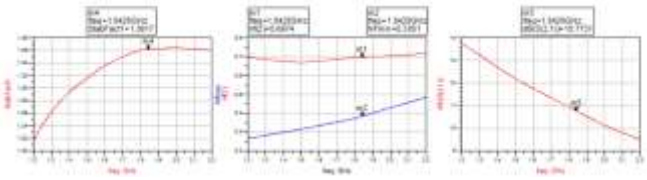

Fig. 8. Simulation result for $C_{blocking}$, C_{bypass} and $L_{blocking}$

Table IV. Value of C and L

Component	Value
$C_{blocking}$	47 pF
C_{bypass}	47 pF
$L_{blocking}$	1 nH

The addition of the Cblocking component to the transistor bias circuit is a DC block so that the DC signal flow as a biasing transistor becomes maximal and is also useful so that the DC signal does not enter the RF port. The addition of the Lblocking component is useful as a DC feed which will block the RF signal so that it does not affect the biasing conditions. And the Cbypass component is useful as a short circuit when an RF signal is flowing in the transistor source area so that the RS is not counted as a load from the transistor.

This study simulates the number of stages of 1-stage, 2-stage, and 3-stage. The simulation result of 1-stage has been already explained above. The design for 2-stage and 3-stage LNA configuration can be seen in Fig. 9 and Fig. 10, respectively. Simulation results for 2-stage and 3-stage can be seen in Fig. 11 and Fig. 12, respectively. Simulation result for 1-stage, 2-stages, and 3-stages can be seen in Table V.

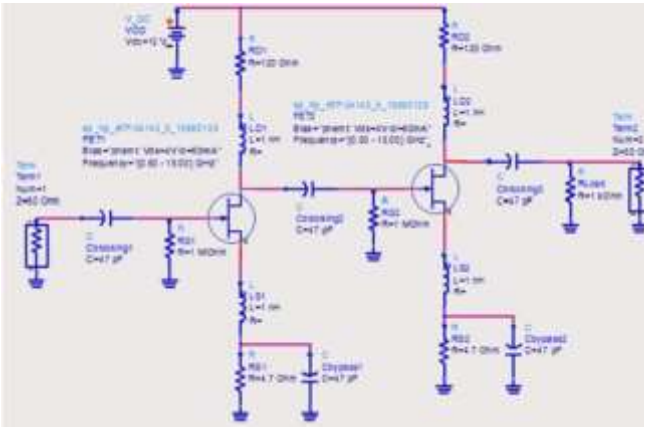

Fig. 9. LNA circuit of 2-stage cascade

The input and output impedance values are searched using a Smith-chart method that can be seen in Fig. 13. Here are the simulation results to get the input and output impedance values, and the configuration of the LNA circuit after the input and output impedances are added. Fig. 14 and Fig. 15 show the step of design the LNA circuit. Fig. 14 show the step of adding an L-network input and output matching circuit. On the addition of this L-Network circuit, the researcher uses component values based on the results of an automatic simulation on the ADS. Fig. 15 shows a final design of 3-stage cascade LNA with a self-bias method.

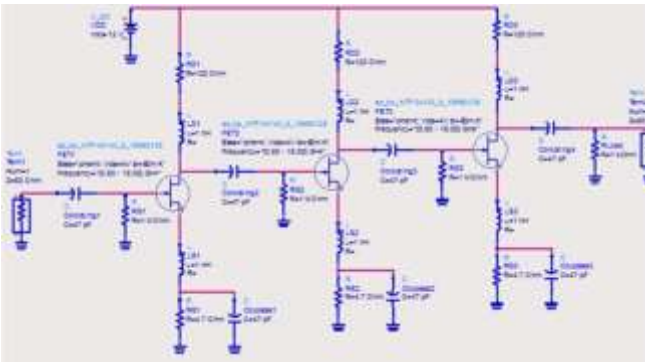

Fig. 10. LNA circuit of 3-stage cascade

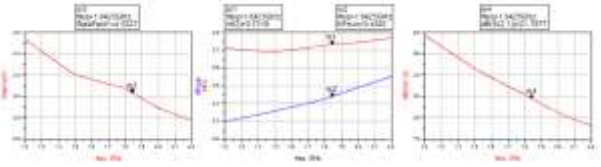

Fig. 11. Simulation result for 2-stage cascade

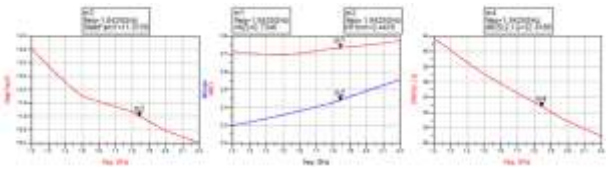

Fig. 12. Simulation result for 3-stage cascade

Table V. Simulation result comparison for LNA with 1-stage, 2-stage, and 3-stage cascade

Specification	Simulation		
	1-stage	2-stage	3-stage
S_{21} (gain)	10.7731 dB	21.7877 dB	32.8166 dB
Noise figure	0.6974 dB	0.7319 dB	0.7346 dB
Stability (K)	1.3617	4.0327	11.0159

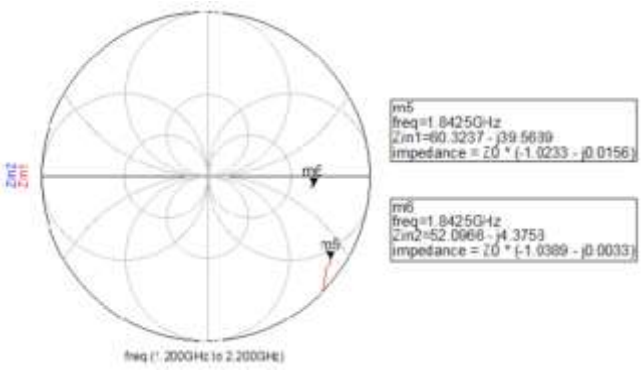

Fig. 13. Input and output impedance simulation result

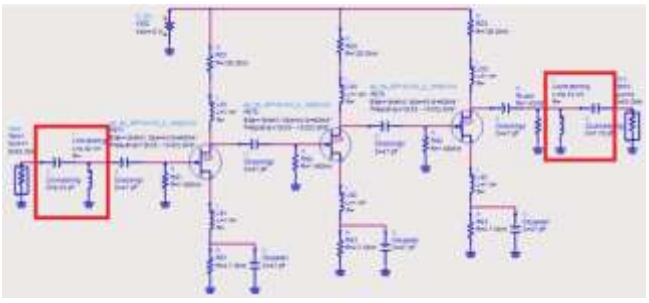

Fig. 14. Step of add an L-network input and output matching circuit

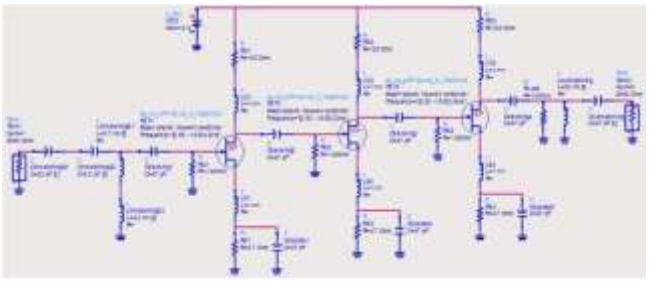

Fig. 15. Final design of 3-stage cascade LNA with self-bias method

IV. RESULT AND DISCUSSION

The most important thing to do in LNA design is to find the right component values so that the LNA meets the expected specifications. Fig.16 and Fig.17 show the simulation results for LNA with a 3-level cascade configuration using self-refraction. Fig. 16 shows the simulation results of input return loss, S11. The input return loss simulation results show that the 3-level cascade configuration LNA has met the expected frequency range specifications of 1.805 - 1.880 GHz with a center frequency of 1.8425 GHz and return loss value is -42.8449 dB. Fig. 17 shows the simulation result of output return loss, S22. The output return loss simulation results show that the 3-level cascade configuration LNA has

met the expected frequency range specifications of 1.805 - 1.880 GHz with a center frequency of 1.8425 GHz and return loss value is -41.3785 dB. Both return loss value meets the return loss requirement value, less than -10 dB.

The simulation result for LNA gain shows in Fig. 18. It shows that the 3-stage cascade configuration LNA design has met the expected gain value specification of more than 18 dB which works at the center frequency of 1.8425 GHz and the resulting gain value is 33.3895 dB. Simulation result for noise figure and stability in 3-stage cascade configuration LNA are shown in Fig. 19 and Fig. 20, respectively. Fig. 19 shows that the noise figure value meets the expected value which is less than 1 dB at the center frequency of 1.8425 GHz and the value is 0,4835 dB. Also for stability, Fig. 20 shows that the stability value is meet the expected value, which is more than 1 at the center frequency of 1.8425 GHz and the value is 11.0159.

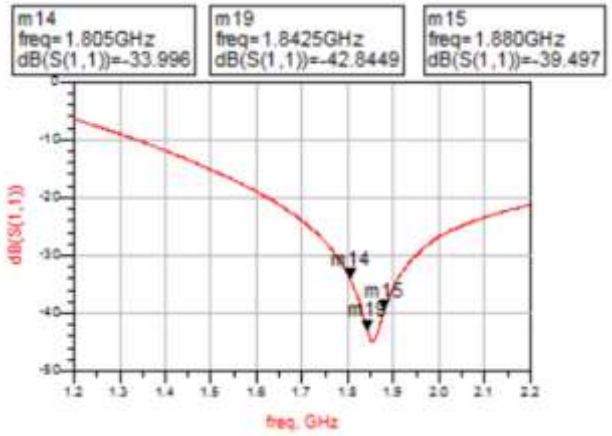

Fig. 16. Input return loss (S_{11}) of LNA design simulation result

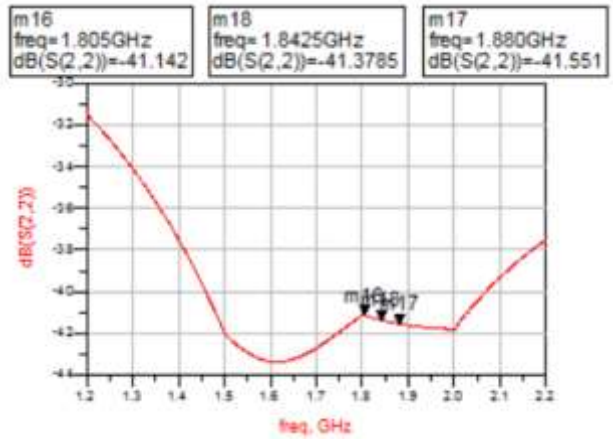

Fig. 17. Output return loss (S_{22}) of LNA design simulation result

In this study, the simulation result for the VSWR value of 3-level cascade configuration LNA meets the expected VSWR value which is less than 2. Fig. 21 shows that the value of input VSWR and the value of output VSWR are 1.0145 and 1.0172, respectively. Both of the VSWR value is for the center frequency of 1.8425. Fig. 22 show the value of input and output impedance. The simulation result shows that the values meet the specification. For the center frequency of 1.8425, the value of input impedance and output impedance are 49.5536 - j0.5617 and 50.8480 + j0.1461, respectively.

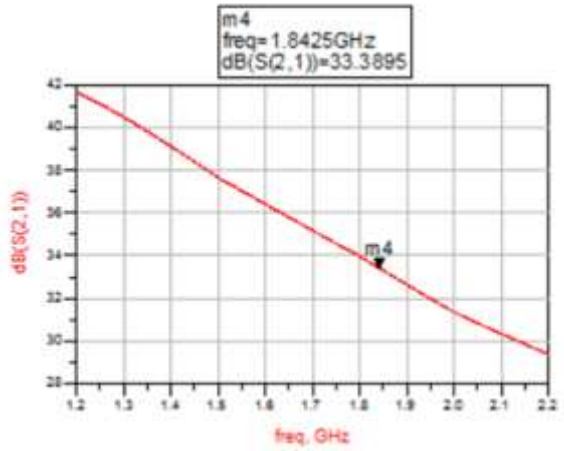

Fig. 18. Gain of LNA design simulation result

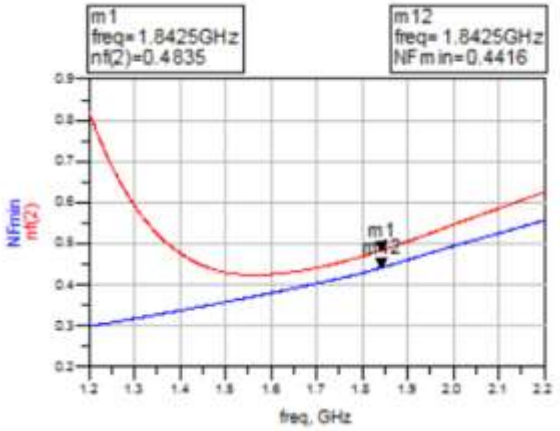

Fig. 19. Noise figure of LNA design simulation result

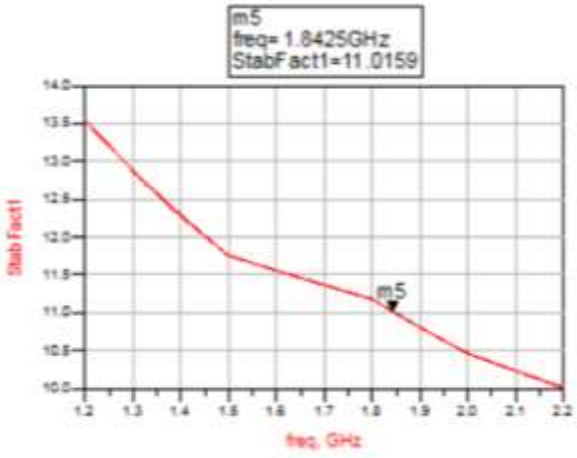

Fig. 20. Stability of LNA design simulation result

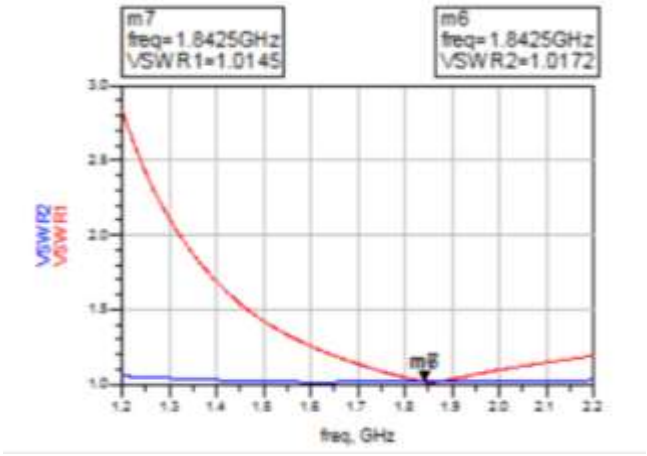

Fig. 21. VSWR of LNA design simulation result.

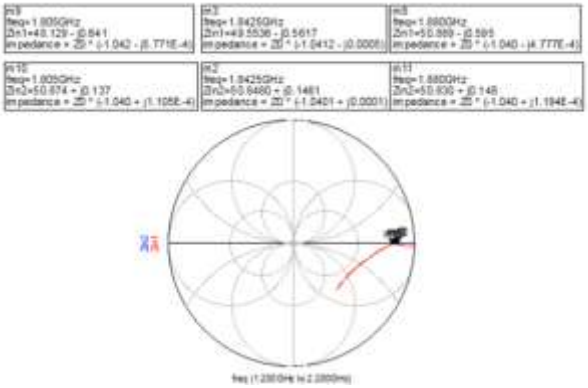

Fig. 22. Input and output impedance of LNA design simulation result

This study also implemented the design simulation to made a physical LNA. Fig. 23 show the dimension of LNA. The measurement results of implemented LNA are shown in Fig. 24, Fig. 25, Fig. 26, Fig. 27, Fig. 28, and Fig. 29. Fig. 24 and Fig. 25 show an input return loss (S11) and input VSWR, respectively. For the input return loss in Fig. 24, the measurement result shows that the value is -7.234 dB at a frequency of 1.724 GHz. For the input VSWR, the value is 5.59 at a frequency of 1.8425 GHz. This value meets the specification that is less than 2.

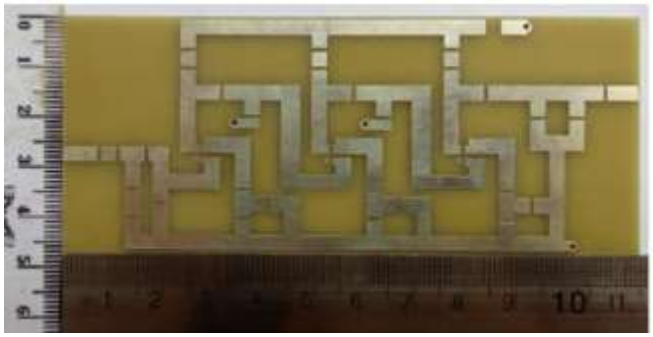

Fig. 23. The implemented LNA

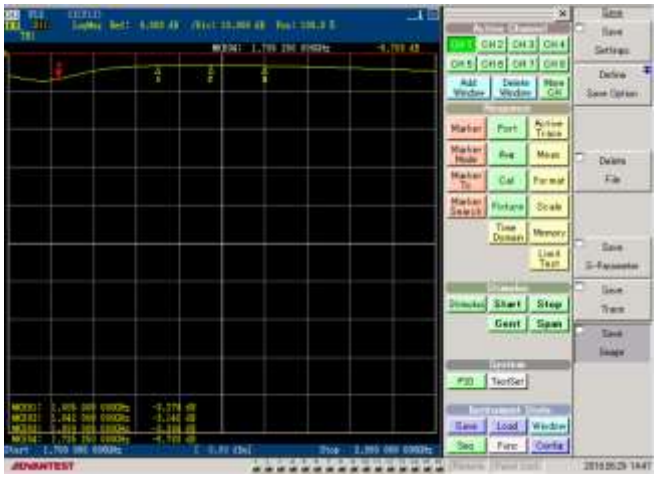

Fig. 24. Measurement result for input return loss (S_{11}) of implemented LNA

Fig. 26 and Fig. 27 show an output return loss (S22) and output VSWR, respectively. For the output return loss in Fig. 26, the measurement result shows that the value is -7.1889 dB at a frequency of 1.8425 GHz. For the output VSWR, the value is 2.552 at a frequency of 1.8425 GHz. This value meets the specification that is less than 2.

For the gain value shown in Fig. 28, the measurement result shows that the gain value is 12.92 dB at a frequency of 1.8425 GHz. In the frequency of 1.735 GHz, the gain value is 19.722 dB. This value meets the specification of LNA that is more than 18 dB.

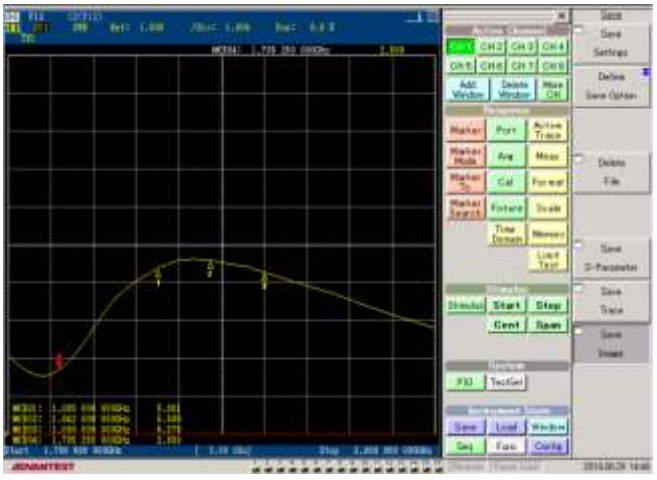

Fig. 25. Measurement result for input VSWR of implemented LNA

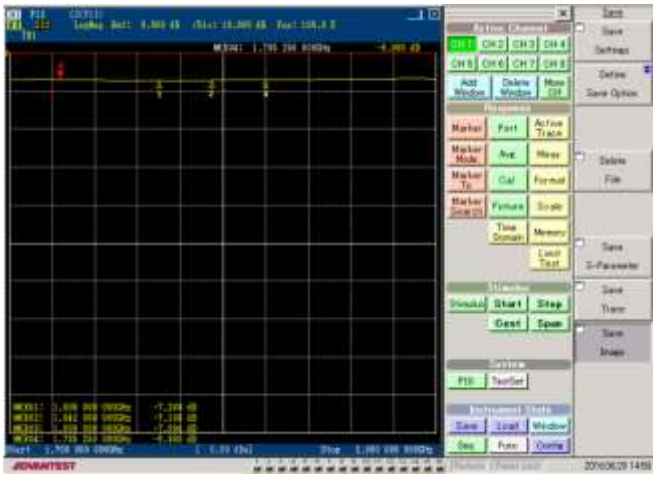

Fig. 26. Measurement result for output return loss (S_{22}) of implemented LNA

Fig. 27. Measurement result for input VSWR of implemented LNA

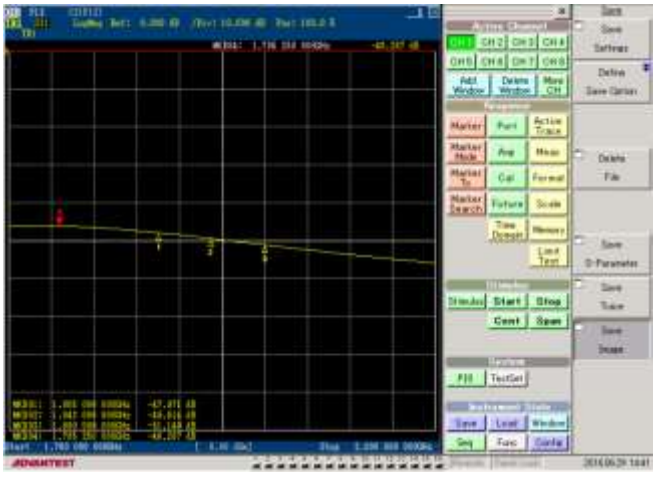

Fig. 28. Measurement result for input gain of implemented LNA

V. CONCLUSION

Develop a Low Noise Amplifier (LNA) for TLE using 3-stage cascade configuration method can produce high gain and improve stability. From the study, the simulation results show that LNA has reached all the expected specification at the frequency of 1805 – 1880 MHz which are gain, input return loss, output return loss, noise figure, VSWR input, and VSWR output are 33.39 dB, -42.85 dB, -41.38 dB, 0.48 dB, 1.01 and 1.02, respectively. The measurement results show that at center frequency LNA obtained value of gain, input return loss, output return loss, VSWR input, and VSWR output as much as 19.72 dB, -6.78 dB, -6.99 dB, 2.69, and 2.62, respectively.

VI. ACKNOWLEDGMENT

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