Optimized Maximum-Swing Gate Diffusion Input Technology for Low Power 1-bit Full Adders

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Abstract— This paper provides a complete swing output for logic 1 and logic 0 for 1-bit complete adder cells and reduces energy consumption, time and field. In its whole configuration, two XOR gate cells and one cell of 2x1 (MUX) multiplexer are used. Compared to various types for complete suppliers by cadency virtuoso simulation on the basis of TSMC 65 nm technology models with a supply voltage of 1v and 125MHz. the output of the proposed version. The results of the simulation showed that the complete adder design proposed disappears from low power and that it increases time and range for all comparative designs.

Keywords— Optimized Gate Diffusion Input (OGDI), Full Adder, Maximum-Swing.

1. INTRODUCTION

Electronic technology is an important part of everybody's life in the modern world of today. The rise in very small appliance density, together with the usage of smartphones and IoT-based computers, require f ast pace, very low power consumption and compactness. New logical circuits / techniques therefore provide low energy consumption and very fast performance. In certain architectures, the simple arithmetic operations like addition , multiplication, and subtraction are used. This can lead to major changes in different algorithms for achieve high speed and low power consumption by efficient implementation. The bulk of this procedure uses a 1-bit complete adder cell as the fundamental building block. This means that the efficiency of the 1-bit adder is improved overall. A variety of complete adder systems contain a number of common logical types and techniques.

The most commonly used CMOS-based complete adder circuit [1] is a 14-PMOS pull-in and a 14- NMOS pull-down system. The architecture contributes to voltage scaling and transistor scale in terms of its exactness. The total swing logic is also encouraged. When executing numerous complex designs, the whole swing rationale is very important[2]. The structure, however, has very high input potential and a wide field. The PMOS transistor is used. In addition, mirror adder is introduced with the rearrangement of the transistors in CMOS architecture [3]. This form of adder leads to a shorter delay in transport than in the CMOS technology [4].

Different researchers are studying the Pass Transistor Logic (PTL) and additional Pass Transistor logic-based complete adders [5, 6].In PTL, the input is connected to the transistor source terminal. While these designs have low surfaces and right restore voltage, they do not have an effective power [7]. It seems that the Gate-Diffusion-Input (GDI) is an alternative strategy containing much of the advantages of the above-mentioned technologies [8]. A complete 1-bit adder based on GDI is therefore provided in this article. The structure is applied by

means of Tanner EDA. The schemas and the architecture are executed and the output parameters are derived by means of a comprehensive post-Layout simulation. The optimized effects are eventually compared with the static CMOS template applied.

Recently, quick advancement in multimedia and digital technologies is very important for the transmission of real-time signals such as audio signal processing, image and video processing. Many technologies, like processors and digital signaling, including filtering and conversion need some form of addition, like multiplication, multiplication and aggregation, and subtraction.

In all these units, the one-bit complete adder cell is the key block [1]. Due to the need for low power consumption in handheld devices like note book and cell phones. Specific considerations in the VLSI architecture are power consumption, limited area of electricity and high speed [2].

The goal of this work was to develop a complete 1-bit adder circuit using full-swing OGDI to decrease power, delay and area, in addition to full-swing outputs. There were several techniques to design in the VLSI circuit, minimizing the power and area.

1.1 INTRODUCTION TO GDI TECHNIQUE

The most critical characteristics for the design of digital circuits are the high performance and restricted field for a digital circuit designer in these days, as well as the minimum power usage in the digital circuit. GDI is a technology that can use digital circuits with limited power interruption. There are one nMOS and one pMOS GDI cells. As with GDI, the sources of the transistor and the respective substrate terminals are irrelevant to supply and can be predicated by chance. The terminals are three: G (shortened gate feedback from nMOS and pMOS). P (pMOS data), and N (nMOS input source). D (a drain terminal with nMOS and pMOS shortened) output [3], 4. Drain terminal. The basic cell of GDI will be shown in fig 2.

Draw Backs of GDI:

1. Output voltage decrease degradation.
2. Excessive energy consumption.
3. NMOS and pMOS are linked to VDD and GND constantly each of them.
4. In standard CMOS process, GDI faces difficulties in manufacturing.

1.2 Modified Gate Diffusion Input (MGDI)

The newest technique in minimum power architecture (MGDI) is the Updated Gate Diffusion Input (MGDI). This method is ideal for fast low voltage circuits with fewer transistors, thereby raising the logical level swing and static power features and making it possible to use small cell library for easy top-down architecture.

The Mod- GDI cell is attached to a high-constant voltage (number pMOS) or vdd (except the PM OS node), input terminals like GDI cell-G (input for drain / source pMOS), P (input to drain / source nMOS), N (input to drain / source nMOS).

The bulk of the NMOS transistor is wired to GND at low constant voltage. For current CMOS production cycles, Mod-GDI cell is suitable [5]. This design of Mod-GDI cells decreases both the sub-threshold and the gate leakage significantly as opposed to the static CMOS switch. The benefits of GDI cells are resolved by MGDI. With the technology scaling, i.e. the linearized 'Y' body coefficient in the lower equation, the influence of the source body voltage on transistor threshold voltage is unnecessary. G, P, N, SP and SN value will continue to be fixed to VDD and GND on a permanent basis.

2. RELATED WORKS

Dagineeshwari, R., & Devadharshini, B. (2020, February). [1] In this research work, a thorough implementation of the 4-bit priority encoder using the modified input gate diffusion technology was proposed. A comparison with the inclusion of CMOS and Updated Gate Diffusion Technological input quality test matrices was conducted on the basis of Cadence 180 nm technology. This is a much higher pace and low power consumption technique.

Radha, N. (2020, July). [2] MGDI is an architectural low capacity design that is a significant change in the Gate diffusion input (GDI) and is the least advanced design approach for fast and low-power models that use a limited transistor number. The proposed 180-nm MGDI technology dependent in the Cadence Virtuoso device is primitive cells-AND, OR, and XOR Gates, full adders, full subtractors, and 4x4 multiplier. GDI's key drawback is that this approach cannot overcome the not enough biased bulk terminal. In order to decrease the number and number of transistors.

Priya, N. S., & Radha, N. (2020, February). [3] An extended, low power-consumption multiplier has been designed to reduce complexity and energy consumption in comparison with other designs. This can speed up and decrease power dissipation. For the implementation of adder configuration, a newer gateway GDI (Gate Diffusion Input) was used. This technology reduces the power consumption, delay and range of low-power digital circuits which therefore face low logic conception problems.

Yadav, H., Goyal, A. K., & Kumar, A. (2020, March). [4] The Gate-Diffusion-Input (GDI) technique implements a 1-bit full adder with a design analysis. Compared with standard static CMOS design the design parameters such as delay, energy consumption, energy delays product, energy and transistor count. Post-layout simulation analyses the effect of parasite capacitance. This shows that the GDI adder's delay and power consumption is around 19% and 94% lower than the CMOS approach together with a decreased number of transistors.

Sarkar, S et al., (2020). [5] It is suggested that a Gate Diffusion Input (GDI) technique be developped to have an 8-bit Arithmetic Logic Unit (ALU). In the ALU architecture, the implementation of GDI technique leads to a low power consumption and a greatly reduced number of transistors. These result in a lower chip area and energy consumption – two of the major digital VLSI design parameters. 3 T XOR is used in the whole adder in this style. In addition, the architecture is also assisted by a new 1-to-8 demultiplexer. Numerous research papers were studied and different logical families were compared, and an 8-bit ALU was finally designed which could perform 8 various operations. The design is validated with the schematical editor DHCH 3.5 and the simulation with Xilinx ISE 14.7 was performed.

Bansal, M., & Singh, J. (2020, September). [6] Use the GDI technique and also 18 nm FinFET is used in analysing simulation results to implement the Vedic multitudinal circuit. The key objective is here to optimise the proposed propagator method, while an analysis consists of parameters such as Delay propagation, Power, Area and Power Delay Product (PDP). The analysis is carried out. The Cadence Virtuoso is used to perform all the studies.

Bansal, M., & Singh, J. (2020, September). [7] The study proposed qualitatively analysed the GDI logic comparator (both 2 bit) using 18 nm FinFET technology, which is used to analyse the CMOS logic stage. Our main objective here is to refine this logical circuitry, such that an experimental analysis is performed which

includes the propagation time, strength, area and power delay product (PDP) parameters. All experimental studies are conducted using Cadence Virtuoso (CDS-FFET 18 nm library).

Yadav, R., & Kumar, M. (2020, February). [8] There is often a zone problem in the design of CMOS circuits to reduce the Gate Diffusion (GDI) technique. Due to this power dissipation, the GDI principle allows to reduce the Transistor Counter (TK). In this report, GDI technology was proposed for the design of a high speed 4x4 Vedic Multiplier. In contrast to traditional CMOS multipliers, the power dissipation of the proposed multiplier is decreased.

Korra ravikumar et al ., (2017). [9] The main objective of this paper is to build the complete adder based on 2T XOR gate with the aid of a GDI technology 2T XOR gate. The strength of the entire adder architecture behind a modern 2T XOR gate system is to reduce the power by counting the transistors with an optimised field.

A. Wagner, A. Fish and A. Morgenshtein. (2002). [10] As an alternative to CMOS logic design, Wagner proposes the Gate Diffusion Input (GDI) technique for the VLSI Digital Design low power silicon region.In reality, this technology proposed the manufacture of insulator silicon (SOI) and CMOS two-well processes. In comparison with CMOS, PTL and TG, it provides an efficient way to design a fast, low-powered design using less transistors. This enables several complex functions to be constructed using only 2 transistors.

This logic style has some limitations, like reduced output voltage swing because of threshold drops, meaning that high or low voltage output is changed by threshold drops from VDD or GND because this decrease in threshold voltage causes a decrease in performance and increases short circuit energy.

The changed gate diffusion logic style (MODGDI) suggested by Morgenshtein, Shwartz and Fish [11] is similar to the basic cell of GDI, but has a major differential in MOD-GDI, GND and VDD substrate terminals, as shown in Figure 1 and 2. This logic is consistent with standard CMOS process implementation and increases performance, power and power delay in contrast to the simple GDI Logic. The problem is not solved but the performance has deteriorated, when the threshold decreases problem.

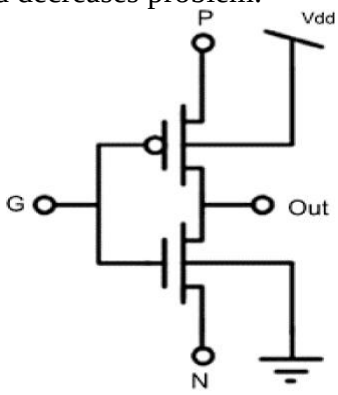

Fig. 1. Modified GDI

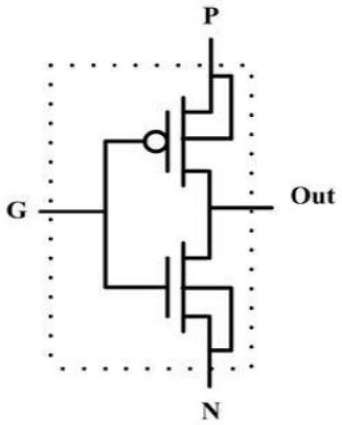

Fig. 2. Basic Gate Diffusion Input

Morgenshtin suggested in [12] a new method that increases the performance swing and overcomes the threshold drop issue known as the Maximum Swing (MS) GDI strategy, using only the swing recover transistor (SR). For the realization of some

logical function, either F1 or F2 gates or a combination of both may be used. While this technique uses more transistors than standard GDI, it uses fewer transistors than standard CMOS logic and achieves full swing performance, low output, less delay and limited circuit field.

3. PROPOSED TECHNIQUE

3.1 XOR Gate

XOR gate is a basic component of multiplier, comparator, adder, decoder and compressor for realising different Digital circuits [6]. The XOR architecture includes 4 transistors as shown in figure 2(a). The performance can be seen as:

$$A \text{ XOR } B = A \oplus B = \overline{A}B + A\overline{B}$$

At A=0, the NMOS transistor is disabled and the PMOS transistor is activated in linear area where PMOS is activated. NMOS is cut off from Vin < VDD, and XOR is cut to (Vtp) the voltage boundary of the PMOS transistor, at Vin-Vtp < Vout < VDD.

At A=0, B=1 NMOS is disconnected from Vin < Vth; PMOS is disconnected from Vin < Vth in the linear area < Vout < VDD; then XOR 's performance equal to VDD passes through PMOS.

The PMOS is disabled at A=1 and the NMO Specifier is allowed whereby PMOS in the linear region Vin > Vtn and NMOS in Vin < Vout < VDD are disconnected and the output of the XOR gate is equivalent to VDD-Vtn, (Vtn) NMOS transistor threshold voltage.

In the linear area of A=1, B= 1 PMOS will be cut and NMOS will be transferred by the NMOS in the equivalent soil. The XOR gate operation in Table I was synthesized. Figure 3 shows the drawbacks of the performance of the NMOS to provide a strong zero in order to solve this problem and Figure 4 shows PMOS to provide strong one in Figure 2(b), wave shape.

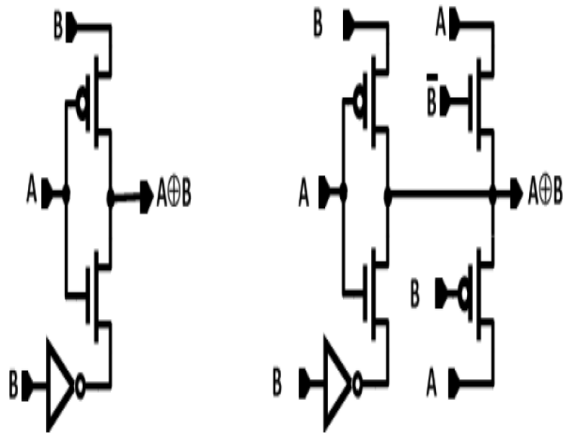

Fig.2. GDI cell; (a) 4T-XOR GATE, (b) 6T-XOR GATE

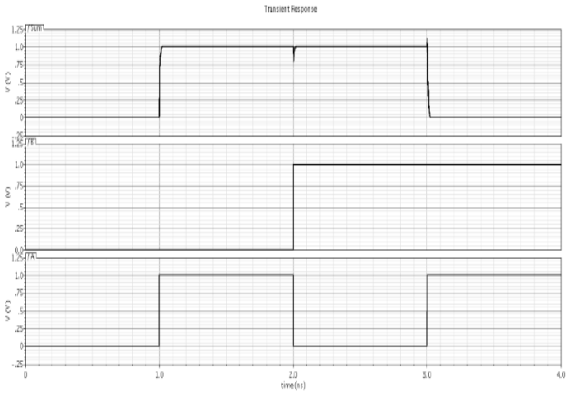

Fig. 3. Waveform of 6T-XOR Gate

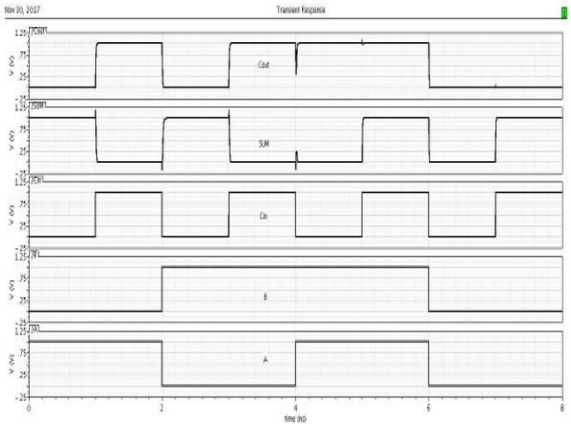

Fig. 4. Output Waveform of the Proposed Design

Table I. Truth Table of XOR Gate.

A	B	A XOR B
0	0	Vtp
0	1	VDD
1	0	VDD-Vtn
1	1	GND

3.2 FULL ADDER

A total adder is a combination circuit that operates 3 bits arithmetically [8]. In addition, the digital signal processing and logic unit was considered an integral feature. The total 1-bit adder comprises three input bits and two output bits, the first two input bits are A and B operands and the third input bit, Cin is brought from a minor point, the effect of the add operation and performance is the result of the input for the next addition operation, and an expression: The full 1-bit adder contains three input bits.

$$\overline{SUM} = A \oplus B \oplus Cin$$

$$COUT = A\,\overline{(A \oplus B)} + Cin\,(A \oplus B)$$

As seen in figure 3, the block diagnosis shown in figure 4 and the table of truth for the complete adder presented in table 2 of the proposed transistors are 16 transistors, including two XOR gate cells, which generate a volume and one multiplexer cell.

Table II Truth Table of Full Adder

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

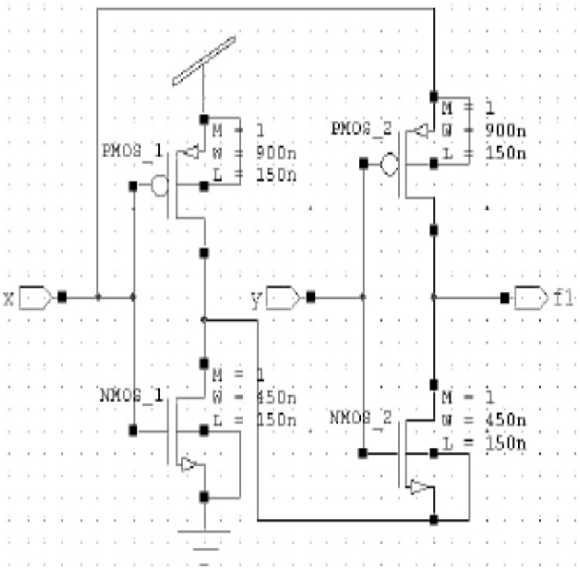

Fig. 3 Schematic design of XOR gate using GDI

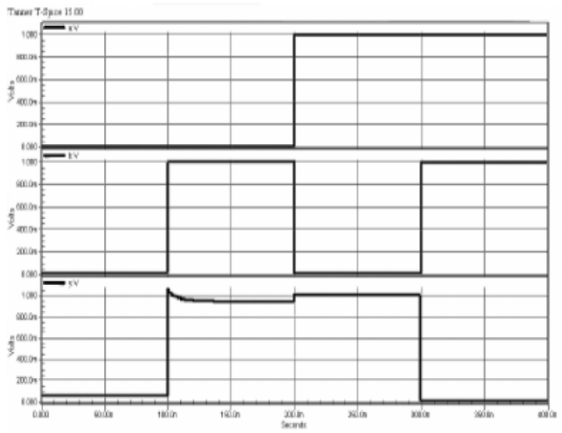

Fig. 4 Waveform of GDI XOR gate

The logic circuit of full adder is shown in the figure given below

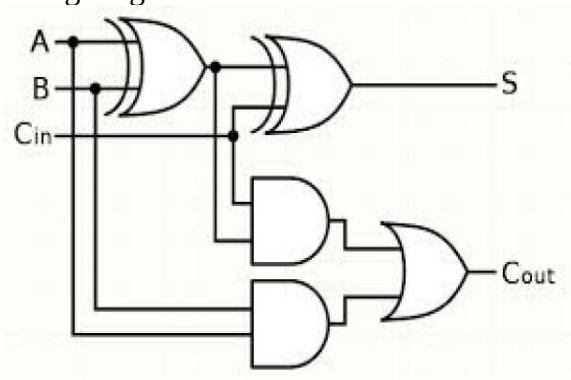

Fig. 5. Logic circuit of full adder

4. SIMULATION RESULTS

The proposed Complete Adder 1-bit circuit was built in a TSMC method of 65 nm. The simulations were performed with SPECTRE dependent Cadence Virtuoso Simulator with a power supply of 1V and a frequency of 125MHz, the transistor NMOS scale of PMOS is double that of Wp / L=240/60, Wn / L=120/60.

Fig.4 describes the Complete Adder waveform. The results of the design suggested in the reference [4], [5] and [6] compared with the previous ones are seen in Table III. Compared with previous designs, the one-bit full adder design is low in power consumption and current full swing performance and lower latency with the smallest number of transistors used for the building circuit.

Table III. Simulation Results

Design	No.of Transistors	Power (nW)	Delay (ps)	Supply Voltage	Techno logy (nm)
[4]	10	693.5	18	1.1	45
[9]	18	5000	45.65	1.2	60
[6]	16	8000	98.45	-	45
[5]	21	927.9	2.5	1	120

5. CONCLUSION

This paper gives a 1-bit Full Adder engineered in 65 nm TSMC process by employing the Full-Swing GDI technique and simulated using the Cadence Virtuoso simulator. Computation analysis indicates design in terms of energy consumption and transmitted power, while allowing strong-Swing Operation. The design concept consists of 16 transistors and continues to operate under 1V supply voltage.

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