A Three-Phase Four-Wire UPQC with Integrated PV Array for Power Quality Enhancement and Voltage Sag Mitigation

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Abstract **– This paper dealt with power quality improvement in power distribution systems by using UPQC with integrated PV array. UPQC is compensating the power quality problems such as voltage unbalances in source side and eliminate the harmonic currents. Such UPQC is connected to the three-phase three wire system or three-phase four wire system. In this paper, PV array will help to improve the duration of the voltage compensation, further DC link voltage rating of the UPQC also reduces. This UPQC consist of dual control strategy. The UPQC contains series and shunt active filters. Series active filter to mitigate voltage disturbances and shunt active filter is to reduce current disturbances simultaneously. Voltage and current controllers are implemented by using synchronous reference frame. A dynamic model of proposed system has been implemented using MATLAB and corresponding results are demonstrating the enhancement of PQ.**

Index Terms – Power quality, Active filters, UPQC, dual control, three-phase distribution.

I. INTRODUCTION

Now-a-days, due to implementation of auto machine and smart technologies for the advantages of mankind, so many power electronic converters are needed to meet requirements. These converters will introduce disturbances like harmonics, sags, swells and distortions which cause a severe impact on the existing system. To mitigate these problems custom power devices were introduced in 20th century. There are several methods have been adopted to mitigate those PQ related disturbances like swell, sag in voltage waveforms and to eliminate harmonics content in the. Initially passive filters are used to mitigate those PQ related issues [1]. Those filters are not applicable to wide range of variations and it was bulky and costly. Further, active filters are leads but those filters are suitable to compensate limited PQ issues only. Now-a-days power electronic devices are connecting in series or shunt or both for mitigating these power quality issues and for increasing the reliability of the supply system including these devices called custom power devices. Custom power devices are Dynamic Voltage Restorer (DVR) also called as series APF [2], Distributed Static Compensator are known as shunt APF and the combination of DVR and DSTAT COM called as Unified Power Quality Conditioner (UPQC).

One of the promising solutions, Unified Power Quality Control was proposed to mitigate the power quality problems of lode side as well as source side. UPQC is used to eliminate harmonics in the current wave form and to control the reactive power requirement of the power system and source voltage issues like sag, swell and improves overall reliability of the power system [2].

DC-link capacitor voltage is mainly influence of compensating all active filters. The magnitude of the phase voltage is always less than the DC link voltage magnitude [2]. The compensation of the source voltage at peak value can also be performing by the DC link voltage capacitor. In addition to dc link voltage in active filters leads to additional stress on the switches of the APF there by making the series APF are very bulky. In general, the ration of dc-link voltage and phase voltage magnitude is about 2.5 [3]. The value of reference current is reduced, when DC link voltage is less than the defined value. Hence, the essential condition for proper compensation of PQ issues is to maintain DC link capacitor voltage greater than the peak amplitude of phase voltage at the PCC [4]. Where as in case of series APF the DC link voltage magnitude should be equal to 1.735 times the peak value of phase voltage.

The value of DC link voltages is distinct for the available APF’s. The ratio of DC link voltage in shunt and series APF’s is about 1.5 times. Two separate dc-link voltages cannot be implemented for a single UPQC topology, suitable value of the dc-link voltage value can be taken for both the active power filters in common. These results to increase in voltages stress on switches of the series active filters, which lead to bulky series active filters [5]. However, a hybrid filters are discussed for motor driving applications. The filters are connected in parallel with diode bridge rectifier for elimination of harmonics. A 3-phase four wire system has more advantage compared with a 3-phase three-wire system. In this topology, neutral clamping is used for the purpose of independent control of each leg of series and shunt active filters. In this paper PV array is used to the UPQC it will improve load voltage compensation can be improved. In this proposed topology consists combination of PV array and UPQC [8].

In this article, configurations of UPQC depending on connections and operations methodologies are discussed in section 2. The control strategy that are that is used in present are discussed in section 3, proposed system simulation model and various results are discussed in section 4, This paper concludes with suitable solutions to compensate the PQ problems which are more available.

II. CONVENTIONAL AND PROPOSED UPQC TOPOLOGIES.

UPQC is able to solve the power quality problems. In Fig 1, UPQC has combined configuration of shunt and series active filters with a common intermediate circuit. Series converter has able to change the harmonic part of source voltage so that the load voltage is sinusoidal and balance [1].

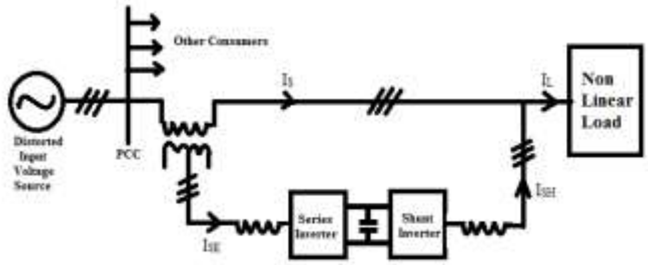

Fig: 1 Configuration of UPQC

The active filter has filtered and limits the harmonics from non-linear loads that the current source is sinusoidal and balance. By adding the power adjustment, without starting sensitive load and without distortion, to compensate reactive unbalanced required by the load. So that, UPQC has work in this condition to compensate shunt or series. In addition, in distribution system was recognized three-phase four wire for energy generation in the three neutral conductor station or transformers with delta-star-delta (Δ-⅄) at the distribution level [10].

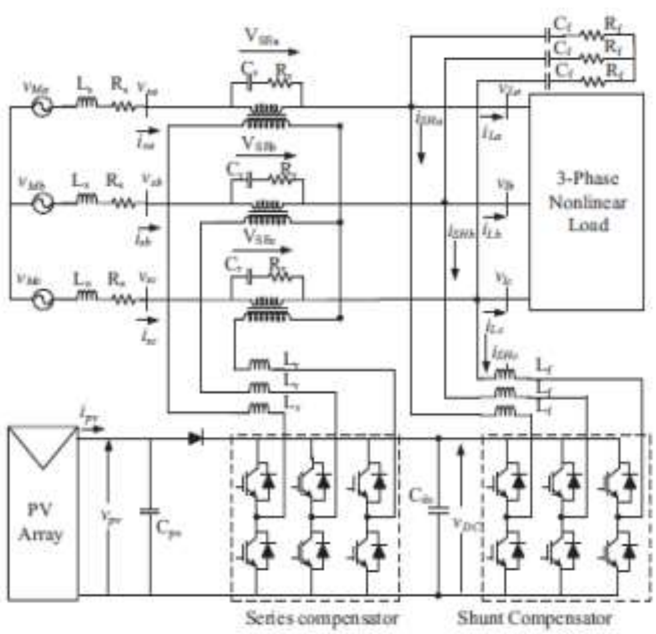

Fig: 2 3P-4W UPQC TERM

Fig 2 shows the conventional UPQC topology was employed with three phase four wire system with neutral clamping [2, 3]. As this neutral clamping method employed independent operation of the each leg and reduced switching count when compared to the existing four leg topology with eight switching are developed [10]. In this proposed topology a series transformer is inject voltage generated by the series compensator into the gird. The use of the ripple filters to filter the generated switching harmonics from converters. The use of the shunt active filter to inject current at the PCC through inductor filter to mitigate the current harmonics and maintain constant voltage across the DC-link.

A. Designing of UPQC parameters

The proposed PV-UPQC system contains two voltage source inverters and a common DC-link capacitor act as source and a PV array, this PV array generates energy to grid as well as elimination of harmonic current in shunt active filters [6]. In this series active power filters compensate the voltage unbalances. Compare with conventional UPQC and proposed UPQC is used for an optimal value of the DC link voltage.

1) Voltage Magnitude of DC-Link:

The voltage magnitude of DC-link voltage V_{dc} depends on the per-phase voltage of the system. The DC-link voltage magnitude is 2 times of the per-phase voltage of the three phase system [13] and is shown as

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ (1)$$

Here, m is modulation is taken as 1 and V_{LL} is the grid voltage value. Line voltage value is 415V, magnitude value of DC-bus voltage is 677.7V the DC-bus voltage is set to be 700V (approx). Which is almost 2 times of the per-phase voltage value of the system.

2) DC-Bus Capacitor Rating: The size of the DC-link capacitor is depend on the power requirement and also DC-bus voltage level. Energy balancing equation for a DC-bus capacitance is given by [13].

$$C_{dc} = \frac{3K_{ka}V_{ph}I_{sh}t}{0.5X(V_{dc}^2 - V_{dc1}^2)}$$

$$= \frac{3X0.2X1.5X239.6X34.5X0.003}{0.5X(700^2 - 677.77^2)}$$

$$= 2200\text{mf} \quad \ldots\ldots\ldots\ (2)$$

Here V_{dc} is the average DC-bus voltage, V_{dc1} is the lowest required value of DC-bus voltage, a is the over load factor, V_{ph} is the per-phase voltage, t is the minimum time required for study value after a disturbance, I_{sh} is per-phase current of shunt compensator, k factor considers in energy during dynamics.

3) Interfacing Inductor for Shunt Compensator: The rating of interfacing inductor of shunt compensator depends upon the current ripples, switching frequency and DC-link voltage value. The equation of interfacing inductor is given by,

$$L_f = \frac{\sqrt{3}m}{12 f_{sh} I_{cr,pp}} V_{dc}$$

$$L_f = \frac{\sqrt{3}X1X700}{12X1.2X10000X6.9} = 1\text{mh} \qquad \text{…….. (3)}$$

Where, m is modulation depth, a is pu value of maximum overload, f_{sh} is switching frequency, $I_{cr,pp}$ is inductor ripple current, it is considered as 20% of rms phase current of shunt compensator. Here, m=1, a=1, f_{sh} =10khz, $V_{dc} = 700v$. The value is approximately 1mh.

III CONTROL OF PV-UPQC

The main control of PV-UPQC is the shunt compensator and the series compensator. The shunt compensator mitigates the power quality problems at load side such as load current harmonics and reactive power compensation. In this proposed PV-UPQC, additional function of shunt compensator is to supply the power from PV array [2, 6]. The shunt compensator supplies power from PV-array by using hysteresis current control. The series compensator mitigates the power quality problems at grid side such as voltage sags/swells by adding additional voltage in phase with grid voltage.

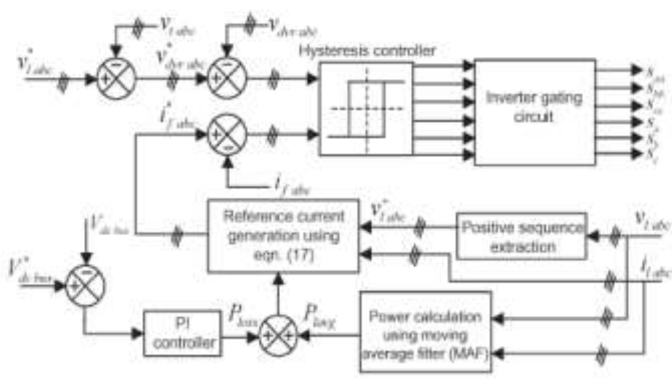

Fig:3 Control Block Diagram for UPQC

In this work, unbalanced and distorted load currents at load side, these currents are flowing through the feeder and make the voltage unbalanced and distorted at terminal. The series active filter makes the balanced and sinusoidal voltage at the PCC. In this case, the voltage contains switching frequency components and it contains some distortion. By using terminal voltage for generating shunt filter current reference [14]. The expression for the reference currents are given by equation (4). In this equation, P_{lavg} is the average load power, P_{loss} denotes the switching loss and ohmic loss in actual compensator voltage PI controller. The term φ is the described phase angle between source voltage and current.

$$i_{fa}^* - i_{la} - i_{sa}^* = i_{la} - \frac{V_{la1}^+ + \Gamma\left(V_{lb1}^+ - V_{lc1}^+\right)}{\Delta_1^+}\left(P_{lavg} + P_{loss}\right)$$

$$i_{fb}^* = i_{1b} - i_{sb}^* = i_{lb} - \frac{V_{lb1}^+ + \Gamma\left(V_{lc1}^+ - V_{la1}^+\right)}{\Delta_1^+}\left(P_{lavg} + P_{loss}\right)$$

$$i_{fc}^* = i_{lc} - i_{sc}^* = i_{lc} - \frac{V_{lc1}^+ + \Gamma\left(V_{la1}^+ - V_{lb1}^+\right)}{\Delta_1^+}\left(P_{lavg} + P_{loss}\right) \quad (4)$$

In this algorithm gives balanced source current after compensation of unbalanced and distorted supply. The series active filter reference voltages are as,

$$V_{dvri}^* = V_{li}^* - V_{ti}$$

$$i = a,b,c \quad \text{....... (5)}$$

Here, V_{li}^* as the desired load voltage in three phases, and V_{dvri}^* is represents the reference series active filter voltage.

The equation for current due to PV array as,

$$I_{pvg} = \frac{2}{3}\frac{P_{pv}}{V_s} \qquad \text{........ (6)}$$

P_{pv} is the pv array power and V_s is the magnitude of the PCC voltage.

In this hysteresis current control is works on feedback loop, generally in two level comparators. Once the reference parameters and the actual parameters are obtained. Voltage source inverter switches are generally used hysteresis current control method [14]. When the error limit exceeds the switching command tolerance band " $\pm h$ ". Usually, the predictive controllers and hysteresis controllers have the more advantageous of peak current limiting capacity and other merits such as extremely good dynamic performance, simplicity in implementation and from independent load parameter variation. The drawback of this hysteresis method is switching frequency of control is highly dependent on the AC voltage and changes it.

The switching commands for the VSI switches are generated from the hysteresis band current control method [11]. Hysteresis current controller is based on a feedback loop with two-level comparators. The switching commands are issued whenever the error limit exceeds a specified tolerance band "±*h*". The hysteresis controller has the advantages of peak current limiting capability, extremely good dynamic performance, and easiness in implementation and independence from load parameter variations. The major disadvantage of the hysteresis band controller is the converter switching frequency is highly dependent on the AC voltage and varies with it.

TABLE 1
SYSTEM PARAMETERS

System parameters	Experimental values
System voltages	230 V (line to neutral), 50 cycles/sec
Feeder impedance	Rs = 1 W; Ls = 10 mH
Non-linear load	3-f full bridge R-L load 150 W and 300 mH
Shunt APF parameters	Cdc = 2200 mF, Lf = 26 mH, Rf = 1 Ω
Series APF parameters	Cse = 80 mF, Lse = 5 mH and Rsw = 1.5 Ω
Injection transformer rating	1:1, 100 V and 700 V
PI controller gains	kp = 6, ki = 5.5
Hysteresis band parameters	h1 = ±0.5 A, h2 = ±6.9 V

A three-phase four-wire supply with a neutral clamped topology is connected to several non-linear loads such as DC motor, induction motor, three-leg diode bridge rectifier and three-leg RL-load. Series and shunt APF are triggered using hysteresis controller. The hysteresis controller senses unbalances in the source voltage and injects the required voltage in phase or out of phase. Corresponding output voltage and current waveforms are plotted.

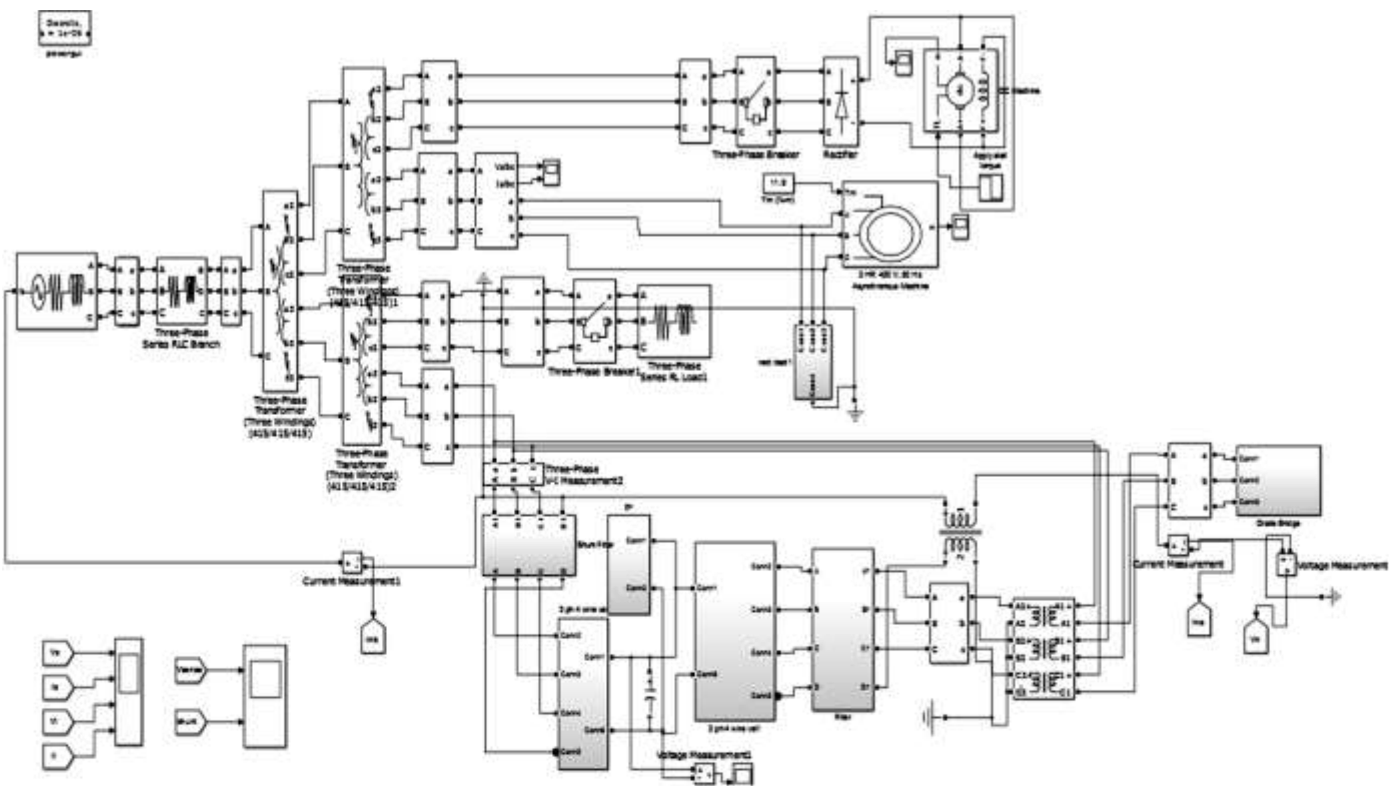

Fig: 4 Simulation circuit of the proposed UPQC topology with PV array

A 3-phase 4-wire UPQC with integrated PV array is connected to non-linear loads of DC-motor, induction motor, 3-leg diode bridge and three-leg RL-load. Series and shunt active filters are designed by using hysteresis controller. In this hysteresis controller detect the unbalanced source voltage and then inject the required voltage in phase or out of phase corresponding output voltage and current waveforms are plotted. By using this topology the DC-link voltage has been reduced from 1060 to700V.

IVSIMULATIONRESULTS

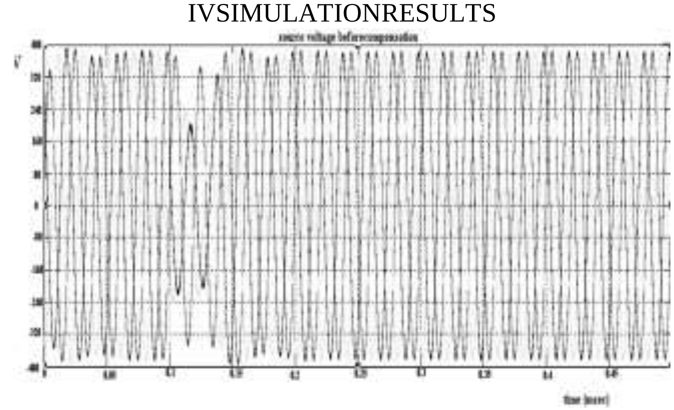

Fig 5: source voltage waveform before compensation

In this Fig 5shows voltage unbalance occurred in 0.1 msec to 0.15 msec due to the sudden switching from the non-linear loads.

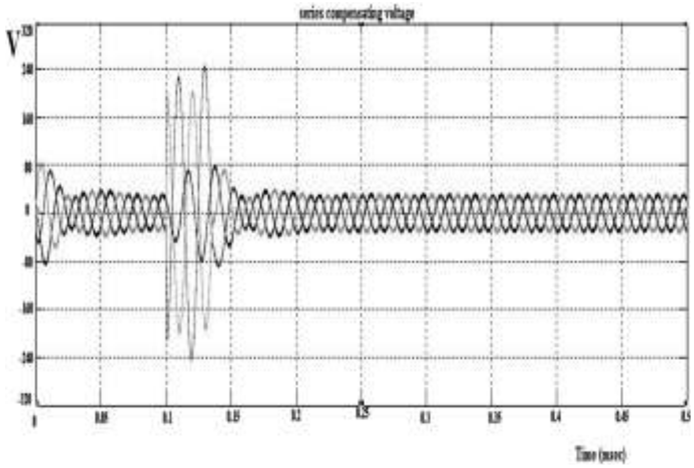

Fig 6: Series injected voltage waveform

In this Fig 6 required voltage for compensating unbalanced voltage is injected during the interval of 0.1 msec to 0.15 msec.

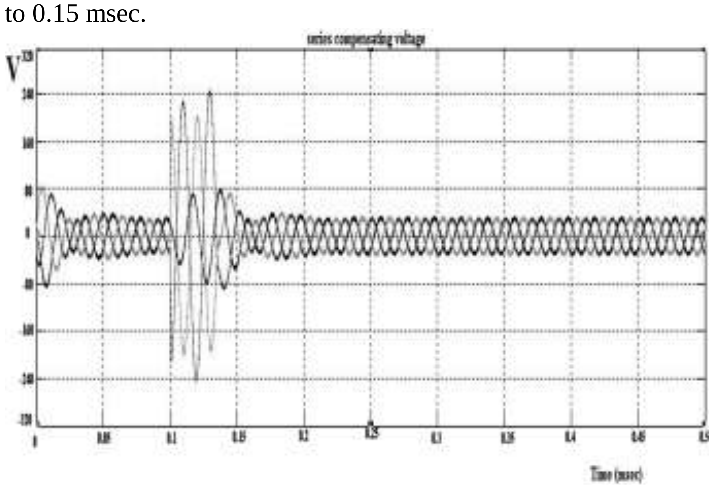

Fig 7: Compensated source voltage.

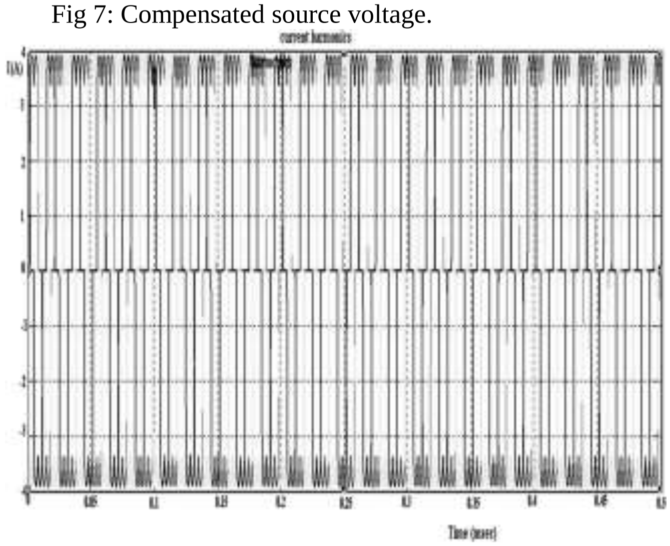

Fig 8: Harmonics in current waveform

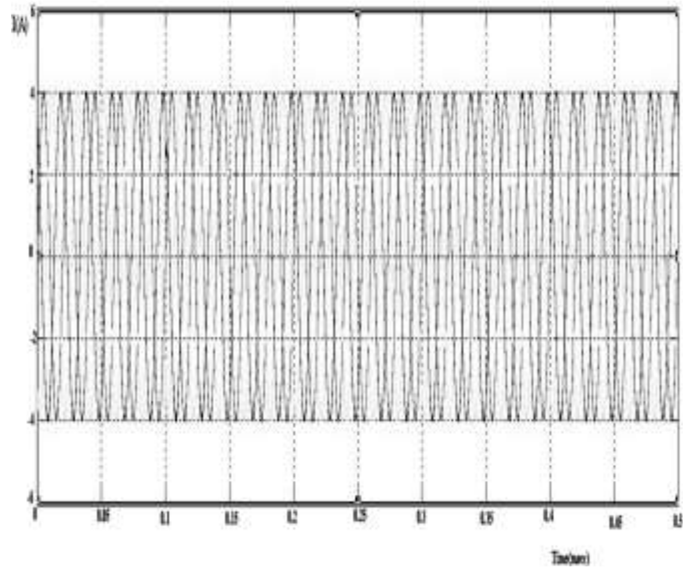

Fig 9: Source current waveform after the elemination of hormonics

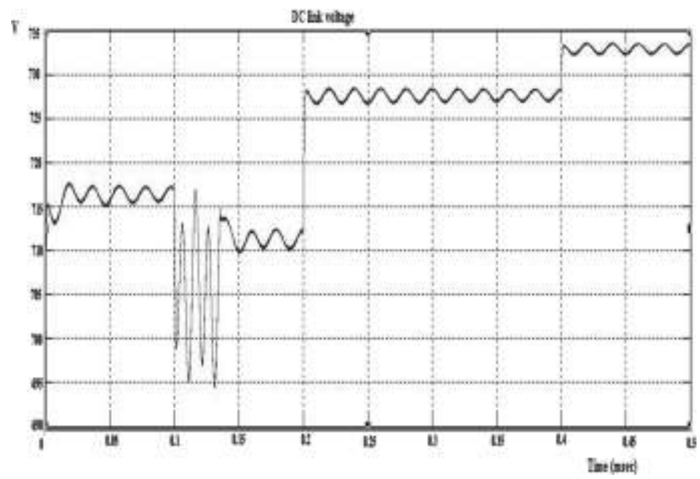

Fig 10: DC-lonk voltage waveform

The simulation results with this proposed topology are shown in above figs. The value of the capacitor (C_f) in the shunt active filter is to be 2mf, and the total dc bus voltage is maintained 700V. The voltage across the capacitor gives to the DC-link voltage are injected the compensated current at the PCC.

V CONCLUSION

In this article, the proposed 3-phase 4-wires UPQC topology with PV array is compensate the voltage sag and harmonic mitigation in load side as well as souse side. The design of C_f, which eliminates and to maintain a common dc-link voltage value for both shunt and series active filters is discussed with the PV array with proposed UPQC system and the results are improving the voltage unbalances for a longer duration of time. A 3-phase 4-wire system with neutral clamping topology has developed for independent operation of the active filters is achieved. This proposal was approved strategy through MATLAB simulation and experimentation view of a distribution system in three phase four wire UPQC with neutral term.

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